Agilent HCPL-270L/ 070L/273L/073L Low Input Current High Gain LVTTL/LVCMOS Compatible 3.3 V Optocouplers

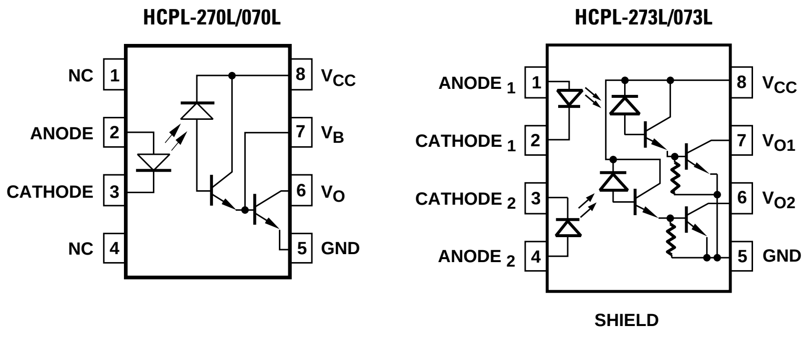
Data Sheet

Description

These high gain series couplers use a Light Emitting Diode and an integrated high gain photodetector to provide extremely high current transfer ratio between input and output. Separate pins for the photodiode and output stage result in LVTTL compatible saturation voltages and high speed operation. Where desired, the V_{CC} and V_O terminals may be tied together to achieve conventional photodarlington operation. A base access terminal allows a gain bandwidth adjustment to be made.

These optocouplers are for use in LVTTL/LVCMOS or other low power applications. A 400% minimum current transfer ratio is guaranteed over 0 to +70°C operating range for only 0.5 mA of LED current.

Functional Diagram



TRUTH TABLE

LED	V_O
ON	LOW
OFF	HIGH

Features

- Low power consumption
- High current transfer ratio
- Low input current requirements – 0.5 mA
- LVTTL/LVCMOS compatible output
- Performance guaranteed over temperature 0°C to +70°C
- Base access allows gain bandwidth adjustment
- High output current – 60 mA
- Safety approval, UL, VDE, CSA (pending)

Applications

- Ground isolate most logic families – LVTTL/LVCMOS
- Low input current line receiver
- High voltage insulation
- EIA RS-232C line receiver
- Telephone ring detector
- 117 V AC line voltage status indicator – low input power dissipation
- Low power systems – ground isolation

A 0.1 µF bypass capacitor connected between pins 8 and 5 is recommended.

CAUTION: It is advised that normal static precautions be taken in handling and assembly of this component to prevent damage and/or degradation which may be induced by ESD.

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The HCPL-070L and HCPL-073L are surface mount devices packaged in an industry standard SOIC-8 footprint.

The SOIC-8 does not require "through holes" in a PCB. This package occupies approximately one-third the footprint area of the standard dual-in-line package. The lead profile is designed to be compatible with standard surface mount processes.

Ordering Information

Specify Part Number followed by Option Number (if desired).

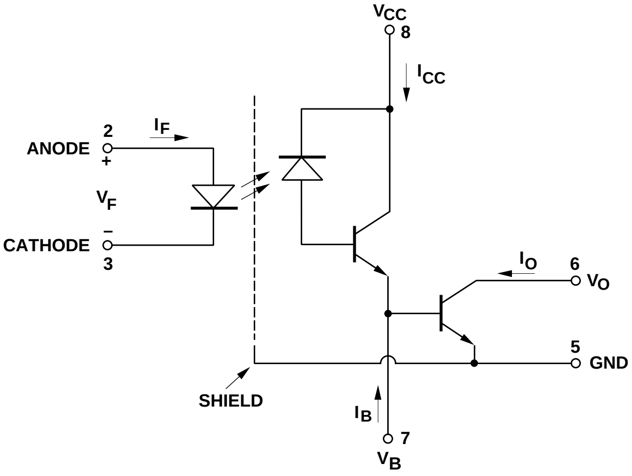
Example:
HCPL-270L #XXX
060 = VDE 0884 V_{IORM} = 630 V_{peak} Option
500 = Tape and Reel Packaging Option

Option data sheets available. Contact your Agilent sales representative or authorized distributor for information.

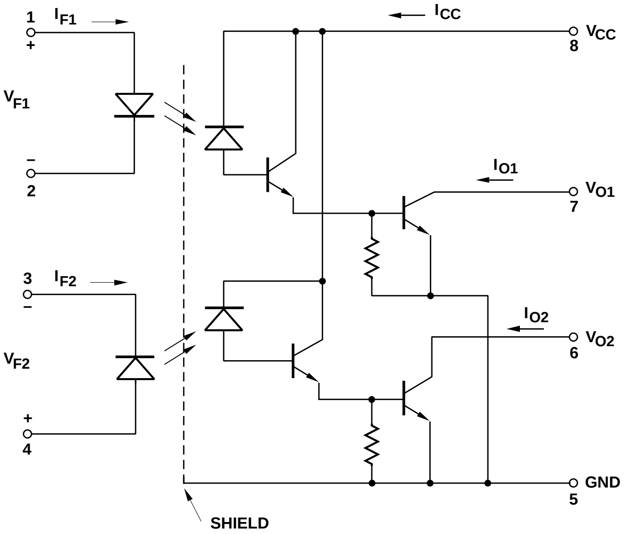
Selection Guide

8-Pin DIP (300 Mil)		Small Outline SO-8			
Single Channel Package HCPL-	Dual Channel Package HCPL-	Single Channel Package HCPL-	Dual Channel Package HCPL-	Minimum Input ON Current (I_F)	Minimum CTR
270L	273L	070L	073L	0.5 mA	400%
				1.6 mA	300%

Schematic



HCPL-270L/HCPL-070L

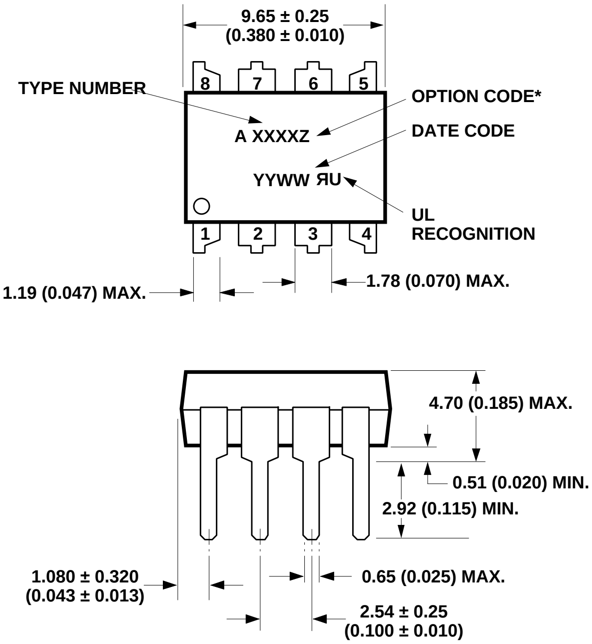


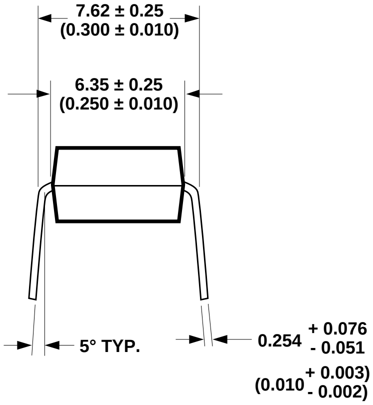
USE OF A 0.1 µF BYPASS CAPACITOR CONNECTED BETWEEN PINS 5 AND 8 IS RECOMMENDED

HCPL-273L/HCPL-073L

Package Outline Drawings

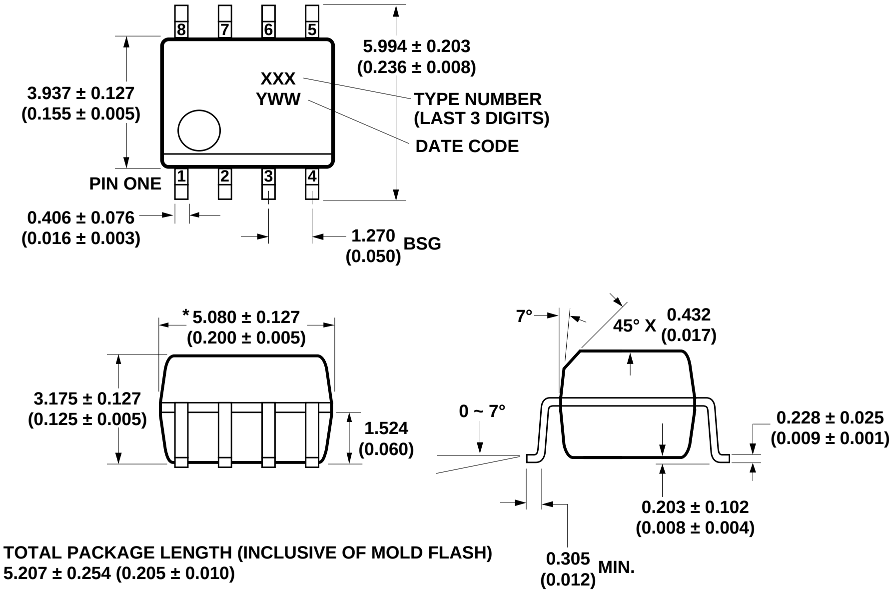
8-Pin DIP Package





DIMENSIONS IN MILLIMETERS AND (INCHES).
*MARKING CODE LETTER FOR OPTION NUMBERS
"L" = OPTION 020
OPTION NUMBERS 300 AND 500 NOT MARKED.

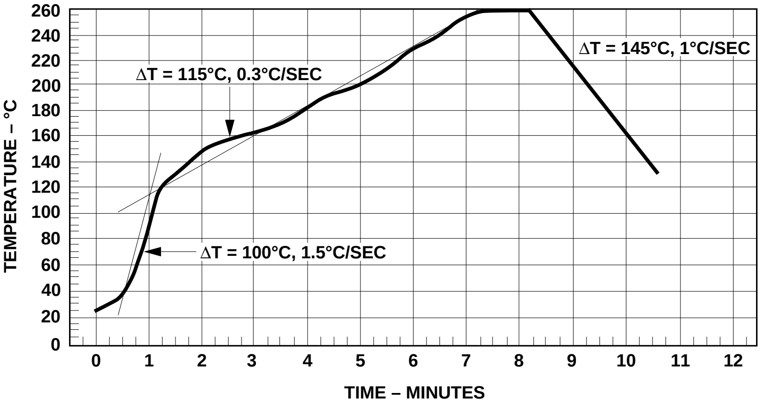
Small Outline SO-8 Package



* TOTAL PACKAGE LENGTH (INCLUSIVE OF MOLD FLASH)
5.207 ± 0.254 (0.205 ± 0.010)

DIMENSIONS IN MILLIMETERS (INCHES).
LEAD COPLANARITY = 0.10 mm (0.004 INCHES) MAX.

Solder Reflow Temperature Profile (Surface Mount Option Parts)



(NOTE: USE OF NON-CHLORINE ACTIVATED FLUXES IS HIGHLY RECOMMENDED.)

Regulatory Information

The devices contained in this data sheet are pending by the following organizations:

UL

Approval (pending) under UL 1577, Component Recognition Program, File E55361.

CSA

Approval (pending) under CSA Component Acceptance Notice #5, File CA 88324.

VDE

Approval (pending) according to VDE 0884/06.92.

Insulation and Safety Related Specifications

Parameter	Symbol	8-Pin DIP (300 Mil) Value	SO-8 Value	Units	Conditions
Minimum External Air Gap (External Clearance)	L (101)	7.1	4.9	mm	Measured from input terminals to output terminals, shortest distance through air.
Minimum External Tracking (External Creepage)	L (102)	7.4	4.8	mm	Measured from input terminals to output terminals, shortest distance path along body.
Minimum Internal Plastic Gap (Internal Clearance)		0.08	0.08	mm	Through insulation distance, conductor to conductor, usually the direct distance between the photoemitter and photodetector inside the optocoupler cavity.
Minimum Internal Tracking (Internal Creepage)		NA	NA	mm	Measured from input terminals to output terminals, along internal cavity.
Tracking Resistance (Comparative Tracking Index)	CTI	200	200	Volts	DIN IEC 112/VDE 0303 Part 1.
Isolation Group		IIIa	IIIa		Material Group (DIN VDE 0110, 1/89, Table 1).

VDE 0884 Insulation Related Characteristics

Description	Symbol	Characteristic	Units
Installation classification per DIN VDE 0110/1.89, Table 1			
for rated mains voltage ≤ 300 V rms		I-IV	
for rated mains voltage ≤ 450 V rms		I-III	
Climatic Classification		55/100/21	
Pollution Degree (DIN VDE 0110/1.89)		2	
Maximum Working Insulation Voltage	V_{IORM}	630	V_{peak}
Input to Output Test Voltage, Method b* $V_{PR} = 1.875 \times V_{IORM}$, 100% Production Test with $t_P = 1$ sec, Partial Discharge < 5 pC	V_{PR}	1181	V_{peak}
Input to Output Test Voltage, Method a* $V_{PR} = 1.5 \times V_{IORM}$, Type and Sample Test, $t_P = 60$ sec, Partial Discharge < 5 pC	V_{PR}	945	V_{peak}
Highest Allowable Overvoltage* (Transient Overvoltage, $t_{ini} = 10$ sec)	V_{IOTM}	6000	V_{peak}
Safety Limiting Values (Maximum values allowed in the event of a failure, also see Figure 11, Thermal Derating curve.)			
Case Temperature	T_S	175	˚C
Current (Input Current I_F, $P_S = 0$)	$I_{S,INPUT}$	400	mA
Output Power	$P_{S,OUTPUT}$	600	mW
Insulation Resistance at T_S, $V_{IO} = 500$ V	R_S	$\geq 10^9$	Ω

*Refer to the front of the optocoupler section of the current catalog, under Product Safety Regulations section, (VDE 0884), for a detailed description.
Note: Isolation characteristics are guaranteed only within the safety maximum ratings which must be ensured by protective circuits in application.

Absolute Maximum Ratings (No Derating Required up to +85˚C)

Parameter	Symbol	Min.	Max.	Units
Storage Temperature	T_S	–55	125	˚C
Operating Temperature	T_A	–40	85	˚C
Average Forward Input Current	$I_{F(AVG)}$		20	mA
Peak Forward Input Current (50% Duty Cycle, 1 ms Pulse Width)	$I_{F(PEAK)}$		40	mA
Peak Transient Input Current (< 1 µs Pulse Width, 300 pps)	$I_{F(TRAN)}$		1.0	A
Reverse Input Voltage	V_R		5	V
Input Power Dissipation	P_I		35	mW
Output Current (Pin 6)	I_O		60	mA
Emitter Base Reverse Voltage (Pin 5-7)	V_{EB}		0.5	V
Supply Voltage and Output Voltage	V_{CC}	–0.5	7	V
Output Power Dissipation	P_O		100	mW
Total Power Dissipation	P_T		135	mW
Lead Solder Temperature (for Through Hole Devices)	260˚C for 10 sec., 1.6 mm below seating plane.			
Reflow Temperature Profile (for SOIC-8 and Option #300)	See Package Outline Drawings section.			

Recommended Operating Conditions

Parameter	Symbol	Min.	Max.	Units
Power Supply Voltage	V_{CC}	2.7	3.3	V
Forward Input Current (ON)	$I_{F(ON)}$	0.5	12.0	mA
Forward Input Voltage (OFF)	$V_{F(OFF)}$	0	0.8	V
Operating Temperature	T_A	0	70	˚C

Electrical Specifications

0°C ≤ T_A ≤ +70°C, 2.7 V ≤ V_{CC} ≤ 3.3 V, 0.5 mA ≤ $I_{F(ON)}$ ≤ 12 mA, 0 V ≤ $V_{F(OFF)}$ ≤ 0.8 V, unless otherwise specified. All typicals at T_A = 25°C. (See Note 8.)

Parameter	Sym.	Device HCPL-	Min.	Typ.*	Max.	Units	Test Conditions		Fig.	Note
Current Transfer Ratio	CTR		400	1300	5000	%	I_F = 0.5 mA	V_{CC} = 3.3 V V_O = 0.4 V	1, 2	2
Logic Low Output Voltage	V_{OL}			0.05	0.3	V	I_F = 1.6 mA, I_O = 8 mA	V_{CC} = 3.3 V		
				0.05	0.4	V	I_F = 5.0 mA, I_O = 15 mA			
Logic High Output Current	I_{OH}			5	25	µA	V_O = V_{CC} = 3.3 V	I_F = 0 mA		2
Logic Low Supply Current	I_{CCL}	270L/070L		0.0015	0.15	mA	V_{CC} = 3.3 V	I_{F1} = I_{F2} = 1.6 mA V_{O1} = V_{O2} = Open		
		273L/073L		0.0015	0.3	mA				
Logic High Supply Current	I_{CCH}	270L/070L		0.002	1	µA	V_{CC} = 3.3 V	I_{F1} = I_{F2} = 0 mA V_{O1} = V_{O2} = Open		
		273L/073L		0.002	2	µA				
Input Forward Voltage	V_F			1.5	1.7	V	T_A = 25°C	I_F = 1.6 mA	3, 4	
Input Reverse Breakdown Voltage	BV_R		5.0			V	I_R = 10 µA, T_A = 25°C			2
Input Capacitance	C_{IN}			60		pF	f = 1 MHz, V_F = 0			2

*All typical values at T_A = 25°C and V_{CC} = 3.3 V, unless otherwise noted.

Switching Specifications (AC)

Over Recommended Operating Conditions (T_A = 0°C to +70°C), V_{CC} = 3.3 V, unless otherwise specified. (See Note 8.)

Parameter	Sym.	Device HCPL-	Min.	Typ.*	Max.	Units	Test Conditions		Fig.	Note
Propagation Delay Time to Logic Low at Output	t_{PHL}					µs	T_A = 25°C		5	2
					30			I_F = 0.5 mA Rl = 4.7 kΩ		
Propagation Delay Time to Logic High at Output	t_{PLH}				90	µs	T_A = 25°C		5	2
								I_F = 0.5 mA, R_L = 4.7 kΩ		
Common Mode Transient Immunity at Logic High Level Output	$\|CM_H\|$		1000	10000		V/µs	I_F = 0 mA, T_A = 25°C, Rl = 2.2 kΩ $\|V_{CM}\|$ = 10 V_{p-p}		6	2, 6, 7
Common Mode Transient Immunity at Logic Low Level Output	$\|CM_L\|$		1000	10000		V/µs	I_F = 1.6 mA, T_A = 25°C, Rl = 2.2 kΩ $\|V_{CM}\|$ = 10 V_{p-p}		6	2, 6, 7

*All typical values at T_A = 25°C and V_{CC} = 3.3 V, unless otherwise noted.

Package Characteristics

Parameter	Sym.	Device HCPL-	Min.	Typ.*	Max.	Units	Test Conditions	Fig.	Note
Input-Output Momentary Withstand Voltage**	V_{ISO}		2500			V rms	RH ≤ 50%, t = 1 min., T_A = 25°C		4, 9
Resistance (Input-Output)	R_{I-O}			10^{12}		Ω	V_{I-O} = 500 Vdc RH ≤ 45%		4
Capacitance (Input-Output)	C_{I-O}			0.6		pF	f = 1 MHz		11
Input-Input Insulation Leakage Current	I_{I-I}		0.005			μA	RH ≤ 45% V_{I-I} = 500 Vdc		5
Input-Input Insulation Leakage Current	R_{I-I}			10^{11}		Ω			5
Capacitance (Input-Input)	C_{I-I}	2730 2731		0.03		pF			5
		0730 0731		0.25					

*All typical values at T_A = 25°C, unless otherwise noted.

**The Input-Output Momentary Withstand Voltage is a dielectric voltage rating that should not be interpreted as an input-output continuous voltage rating. For the continuous voltage rating refer to the VDE 0884 Insulation Characteristics Table (if applicable), your equipment level safety specification or Agilent Application Note 1074 entitled "Optocoupler Input-Output Endurance Voltage."

Notes:

1. Pin 5 should be the most negative voltage at the detector side.
2. Each channel.
3. DC CURRENT TRANSFER RATIO (CTR) is defined as the ratio of output collector current, I_O, to the forward LED input current, I_F, times 100%.
4. Device considered a two-terminal device: pins 1, 2, 3, and 4 shorted together, and pins 5, 6, 7, and 8 shorted together.
5. Measured between pins 1 and 2 shorted together, and pins 3 and 4 shorted together.
6. Common mode transient immunity in a Logic High level is the maximum tolerable (positive) dV_{CM}/dt of the common mode pulse, V_{CM}, to assure that the output will remain in a Logic High state (i.e., $V_O > 2.0$ V). Common mode transient immunity in a Logic Low level is the maximum tolerable (negative) dV_{CM}/dt of the common mode pulse, V_{CM}, to assure that the output will remain in a Logic Low state (i.e., $V_O < 0.8$ V).
7. In applications where dV/dt may exceed 50,000 V/μs (such as static discharge) a series resistor, R_{CC}, should be included to protect the detector IC from destructively high surge currents. The recommended value is R_{CC} = 110 Ω.
8. Use of a 0.1 μF bypass capacitor connected between pins 5 and 8 adjacent to the device is recommended.
9. In accordance with UL 1577, each optocoupler is proof tested by applying an insulation test voltage > 3000 V rms for 1 second (leakage detection current limit, $I_{I-O} < 5$ μA).
10. In accordance with UL 1577, each optocoupler is proof tested by applying an insulation test voltage > 6000 V rms for 1 second (leakage detection current limit, $I_{I-O} < 5$ μA).
11. Measured between the LED anode and cathode shorted together and pins 5 through 8 shorted together.
12. Derate linearly above 65°C free-air temperature at a rate of 2.3 mW/°C for the SO-8 package.

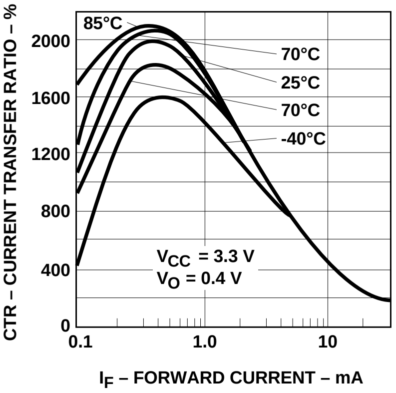


Figure 1. Current transfer ratio vs. forward current.

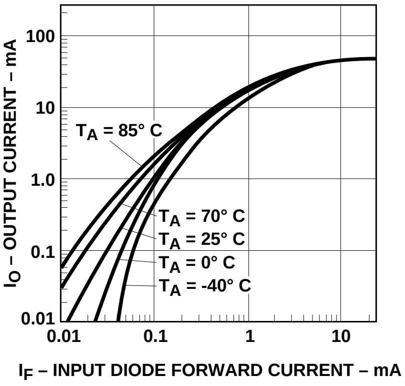


Figure 2. Output current vs. input diode forward current.

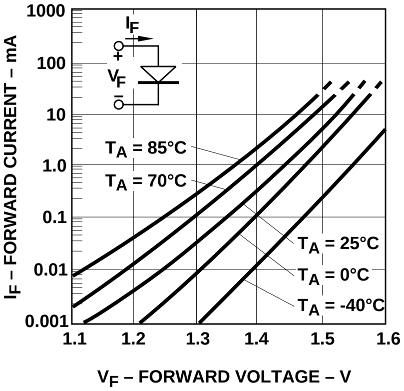


Figure 3. Input diode forward current vs. forward voltage.

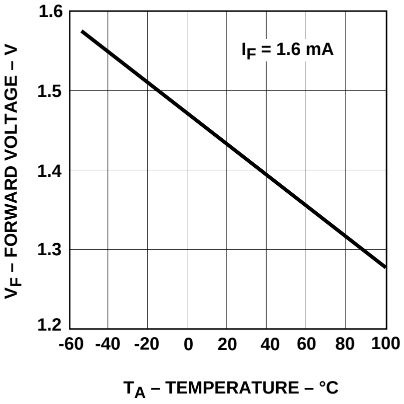


Figure 4. Forward voltage vs. temperature.

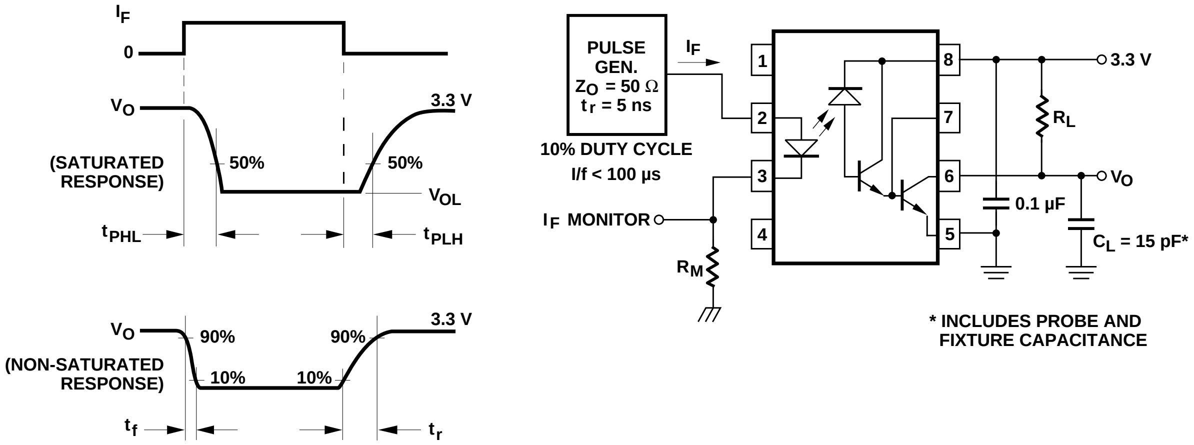


Figure 5. Switching test circuit.

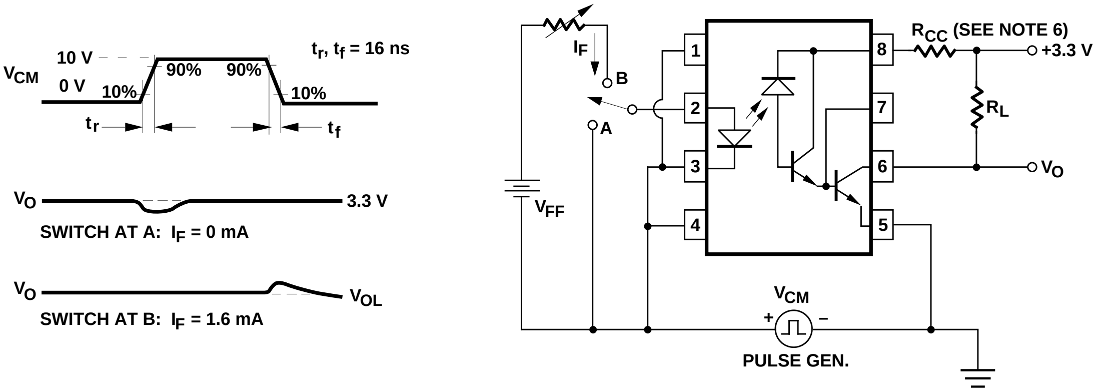


Figure 6. Test circuit for transient immunity and typical waveforms.

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