

Description:

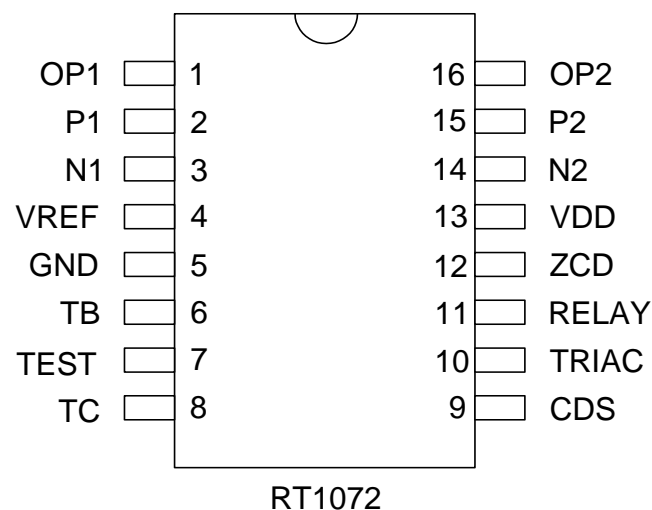
RT1072 IS A PIR (Passive Infra-Red) CONTROLLER; THE PIR CONTROLLER CAN SENSE THE MOTION MOVEMENT AND ACTIVATE THE ELECTRONIC APPLICATION. THE INTERSTRUCTURE OF THE PIR CONTROLLER IC IS USING THE ANALOG MIXING DIGITAL TECHNIQUE TO DESIGN (MIXED-MODE); IT IS PROVEN TO BE VERY STABLE IN ANY CIRCUMSTANCES. IT CAN BE EITHER DRIVE TRIAC OR RELAY DEPENDING ON USERS' CHOICE. THE APPLICATION CIRCUIT IS VERY COST EFFECTIVE.

FEATURES :

1. MIXED-MODE CMOS IC.
2. HIGH NOISE IMMUNITY.
3. CONSTANT CURRENT CDS INPUT.
4. PIR INPUT.
5. ADJUSTABLE OUTPUT DURATION.
6. DRIVE EITHER RELAY OR TRIAC.

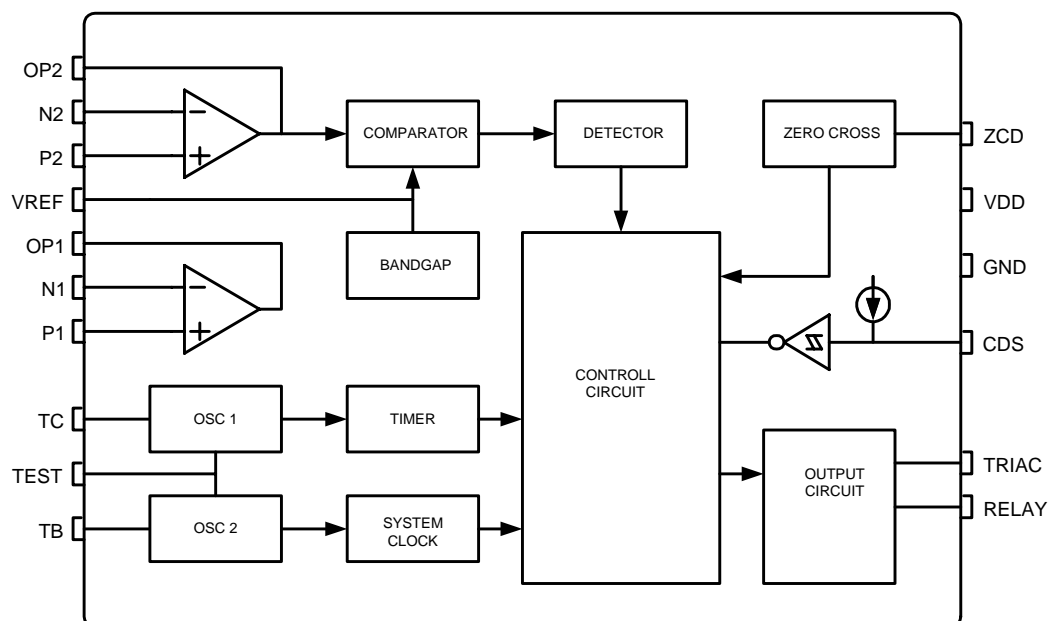
APPLICATION :

1. HOME, OFFICE OR FACTORY SECURITY SYSTEMS.
2. AUTO LIGHTING SYSTEMS.
3. AUTO DOOR BELL.
4. MOTION DETECTOR.

PIN CONFIGURATION :

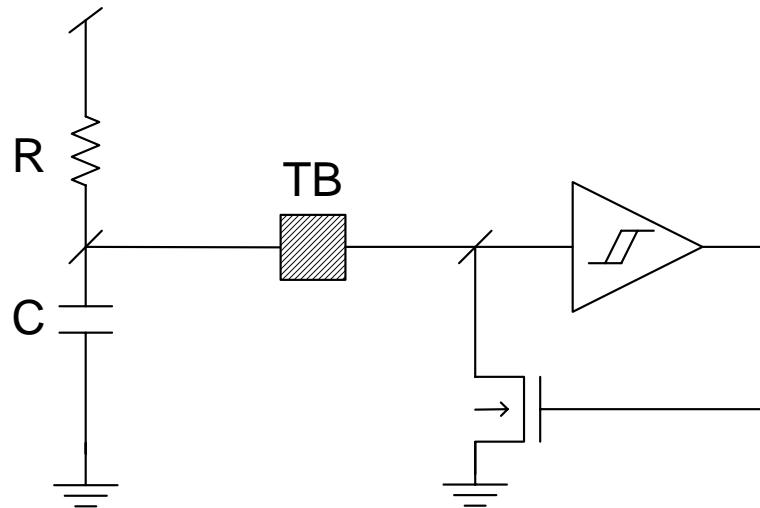
PIN DESCRIPTION :

PIN No.	PIN Name	I/O	Description
1	OP1	O	FIRST STAGE OP OUTPUT.
2	P1	I	FIRST STAGE OP POSITIVE INPUT.
3	N1	I	FIRST STAGE OP NEGATIVE INPUT.
4	VREF	O	REGULATOR VOLTAGE.OUTPUT
5	GND		GROUND.
6	TB	I	EXTERNAL R.C.OSCILLATION CIRCUIT FOR SYSTEM FREQUENCY.
7	TEST	I	IC TEST PIN.
8	TC	I	EXTERNAL R.C.OSCILLATION CIRCUIT TO ACTIVATE THE TIMING OF TRIAC OR RELAY.
9	CDS	I	TO CONNECT TO CDS SENSOR. TO SENSE THE SURROUNDING DARK & BRIGHTNESS.
10	TRIAC	O	WHEN THE SYSTEM IS ACTIVATING, THE SIGNAL WILL ACTIVE LOW TO DRIVE TRIAC.
11	RELAY	O	WHEN THE SYSTEM IS ACTIVATING, THE SIGNAL WILL ACTIVE HIGH TO DRIVE APPLICATION CIRCUIT OF RELAY.
12	ZCD	I	DETECT ZERO CROSS OF AC LINE
13	VDD		POSITIVE POWER INPUT
14	N2	I	2 ND STAGE OP NEGATIVE INPUT.
15	P2	I	2 ND STAGE OP POSITIVE INPUT.
16	OP2	O	2 ND STAGE OP OUTPUT.

FUNCTIONAL DESCRIPTION :**Block Diagram :**

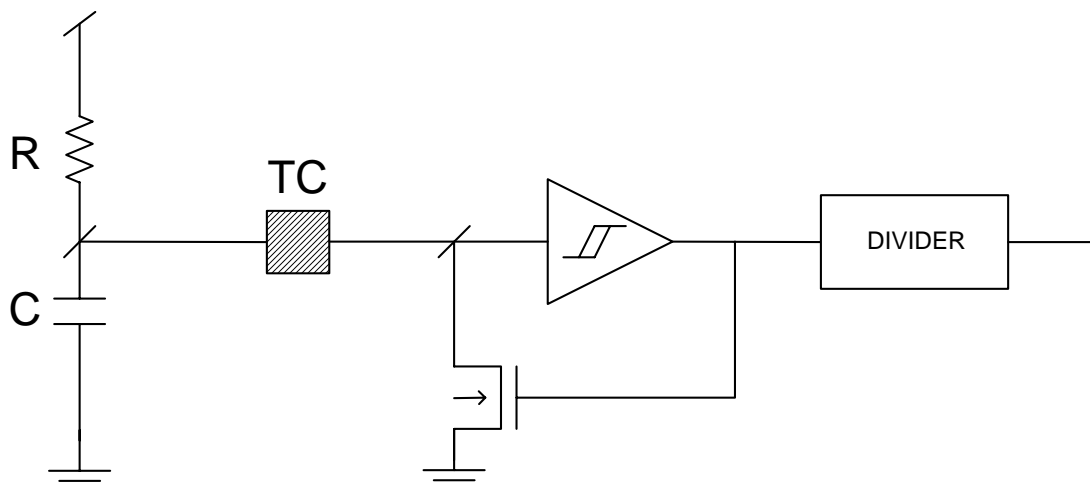
TB :

WHEN THE PIR DETECT A SIGNAL INPUT, THE SIGNAL SHOULD BE LARGER THAN 768 TB CYCLE. AND THE SYSTEM WILL RECOGNISED THE SIGNAL, AFTER THE RECOGNITION IS ACCEPTED, AND SYSTEM WILL DELAY 32 TB CYCLE, AND IT WILL SENT A PULSE TO ACTIVATE EITHER TRIAC OR RELAY. WHEN THE TRIAC OR RELAY CHANGES FROM ACTIVE INTO INACTIVE MODE, THE SYSTEM HAVE TO GO THROUGH 4096 TB CYCLE TO DETECT ANOTHER PIR SIGNAL AGAIN.



TC :

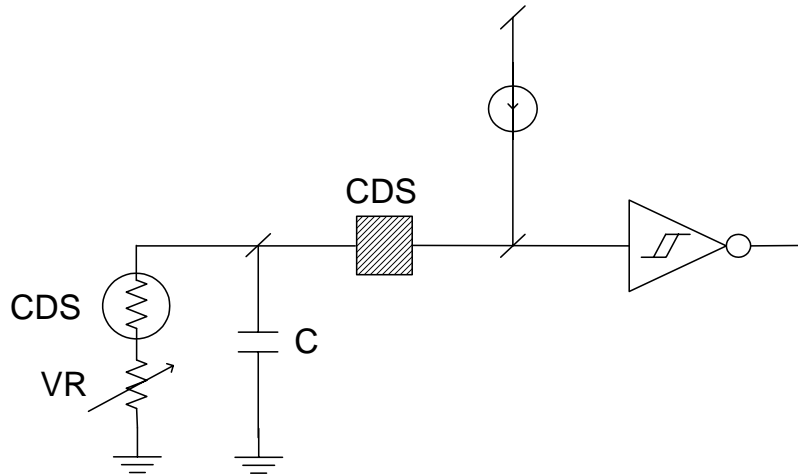
WHEN THE SYSTEM IS ACTIVATE, TRIAC OR RELAY WILL CONTINUOUSLY SENT OUT A SIGNAL, THE TIMING OF THE SIGNAL CAN BE SET BY TC, THE TOTAL TIMING PERIOD FOR TC CYCLE IS 245760. THE PERIOD OF TC CAN BE TUNE BY RC. DURING THE ACTIVE PERIOD, IF THE SYSTEM RECEIVES THE PIR SIGNAL, THEN IT RESTARTS COUNTING THE TIMING BEGIN WITH 245760 AGAIN.



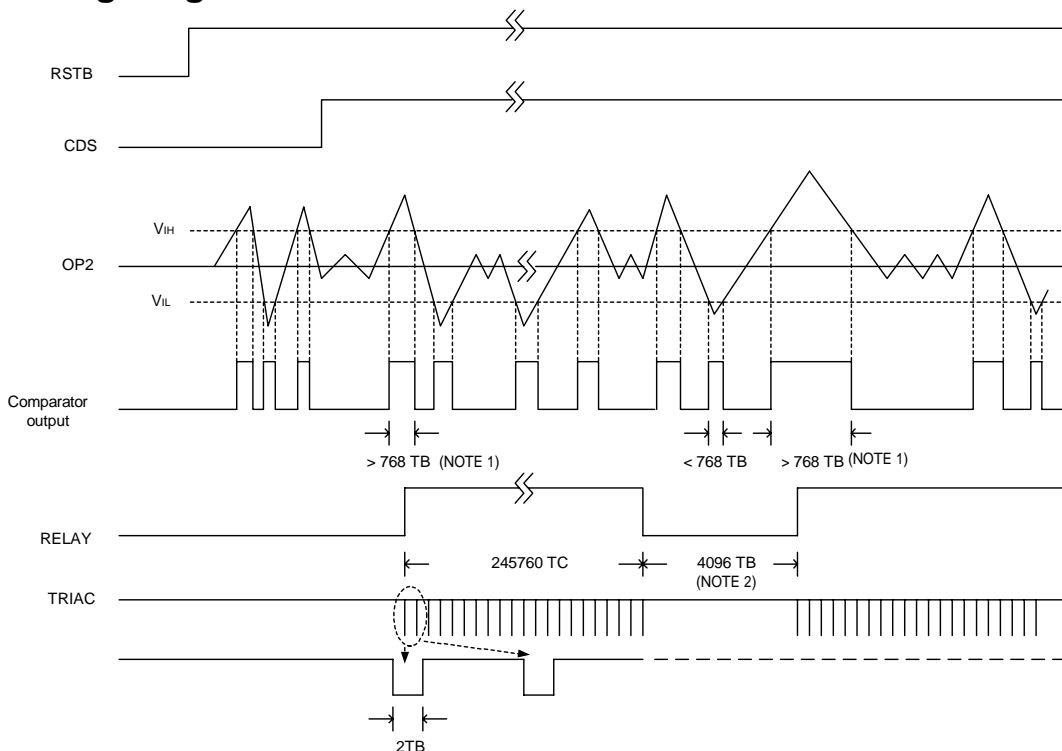
CDS :

THE INPUT PIN IS TO DETECT DAY OR NIGHT, IF THE BRIGHTNESS IS BRIGHT ENOUGH, THE CDS WILL REMAIN IN LOW STATE, THE PIR IS NOT ACTIVATE, THE OTHER HAND, CDS WILL IN HIGH STATE AND ENABLE CDS FUNCTION.

ON



Timing Diagram :



NOTE : (一)COMPARATOR OUTPUT SIGNAL SHOULD BE LARGER THAN 768 TB CYCLE, THEN THE SYSTEMS IS ACTIVATE, IF NOT, IT WILL DEACTIVATE.
(二)TRIAC OR RELAY OUTPUT CONTINUOUS ACTIVE PERIOD IS 245760 TC CYCLE, DURING THE ACTIVE PERIOD, IF THE SYSTEM RECEIVES ANOTHER PIR SIGNAL, THEN IT RESTARTS COUNTING THE TIMING UNTIL IT IS OVER.

Maximum Ratings

Symbol	Parameter	Condition	Rating	Unit
V_{DD}	Supply voltage		-0.3 ~ 6	V
V_I	Input voltage		-0.3 ~ $V_{CC}+0.3$	V
V_O	Output voltage		-0.3 ~ $V_{CC}+0.3$	V
P_{dis}	Max. Power Dissipation	$V_{DD}=5V$	300	mW
T_{OP}	Operating Temperature		-20 ~ 70	
T_{st}	Storage Temperature		-50 ~ 125	

Electrical Characteristics

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
V_{DD}	Supply voltage		3.6	5	5.5	V
V_{ref}	Regulated Voltage	$V_{DD}=5V$	3	3.2	3.4	V
$V_{IH(CDS)}$	CDS Input High Voltage	$V_{DD}=5V$	2.1	2.3	2.5	V
$V_{IL(CDS)}$	CDS Input Low Voltage	$V_{DD}=5V$	1.5	1.7	2.0	V
I_{DD}	Operating Current	$V_{DD}=5V$ No Load, OSC ON	60	70	100	μA
I_{SB}	Stand By Current	$V_{DD}=5V$ No Load, OSC OFF		40	60	μA
I_{ref}	Source Current of V_{ref}		200			μA
I_{CDS}	Source Current of CDS		3	5	10	μA
$I_{OH(relay)}$	Source Current of Relay				5	mA
$I_{OL(relay)}$	Sink Current of Relay				5	mA
$I_{OL(triac)}$	Sink Current of TRIAC				15	mA
f_{TB}	Frequency of TB		12.8	16	19.2	KHz
f_{TC}	Frequency of TC		12.8	16	19.2	KHz
A_{VO}	OP Amp open loop gain	$V_{DD}=5V$		100		dB
V_{OS}	OP Amp Input offset voltage	$V_{DD}=5V$			5	mV