



Features

- Low On-resistance 8 ohms
- Breakdown voltage 350V minimum
- High input impedance
- Low input and output leakage
- Small package size SOT-223
- PC Card (PCMCIA) Compatible
- PCB Space and Cost Savings

Applications

- Support Component for LITELINK™ Data Access Arrangement (DAA)
- Telecom

Description

The CPC5602C is an “N” channel depletion mode Field Effect Transistor (FET) that utilizes Clare’s proprietary third generation vertical DMOS process. The third generation process realizes world class, high voltage MOSFET performance in an economical silicon gate process. The vertical DMOS process yields a highly reliable device particularly in difficult application environments such as telecommunications.

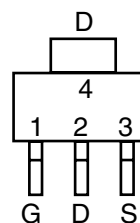
One of the primary applications for the CPC5602C is as a linear regulator/ hook switch for the LITELINK family of Data Access Arrangements (DAA) Devices CPC5610A, CPC5611A, CPC5620A, CPC5621A, and CPC5622A.

The CPC5602C has a typical on-resistance of 8Ω, a breakdown voltage exceeding 350V and is available in an SOT-223 package. As with all MOS devices, the FET structure prevents thermal runaway and thermal-induced secondary breakdown.

Ordering Information

Part Number	Description
CPC5602C	N-Channel Depletion Mode FET, SOT-223 Package (80/tube)
CPC5602CTR	N-Channel Depletion Mode FET, SOT-223 Package Tape and Reel (1000/reel)

Package Pinout



Pin Number	Name
1	GATE
2	DRAIN
3	SOURCE
4	DRAIN

Absolute Maximum Ratings

Parameter	Min	Max	Units
V_{DS} Voltage	-	350	V
Total Package Dissipation	-	2.5	W
Operational Temperature	-40	+85	°C
Storage Temperature	-40	+125	°C

Electrical absolute maximum ratings are at 25°C

Absolute Maximum Ratings are stress ratings. Stresses in excess of these ratings can cause permanent damage to the device. Functional operation of the device at conditions beyond those indicated in the operational sections of this data sheet is not implied.

Electrical Characteristics (@25°C unless otherwise specified)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Breakdown Voltage	$V_{(BR)DS}$	-	350	-	-	V
Gate-to-Source Off Voltage	$V_{GS(off)}$	$I_D = 2\mu A$, $V_{DS}=10V$, $V_{DS}=100V$	-3.6	-	-2	V
Drain-to-Source Leakage Current	$I_{DS(off)}$	$V_{GS} = -5V$, $V_{DS}=190V$	-	-	20	nA
		$V_{GS} = -5V$, $V_{DS}=350V$	-	-	1	μA
Drain Current	I_D	$V_{GS} = -2.7V$, $V_{DS}=5V$, $V_{DS}=50V$	-	-	5	mA
		$V_{GS} = -0.57V$, $V_{DS}=5V$	130	-	-	mA
On Resistance	$R_{DS(on)}$	$V_{GS} = -0.35V$, $I_{DS}=50mA$	-	8	14	Ω
Gate Leakage Current	I_{GSS}	$V_{GS}=10V$, $V_{GS}=-10V$	-	-	0.1	μA
Gate Capacitance	C_{ISS}	$V_{DS} = V_{GS}=0V$	-	-	300	pF

Thermal Characteristics

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Thermal Resistance	$R_{\theta JC}$	-	-	-	14	°C/W

Manufacturing Information

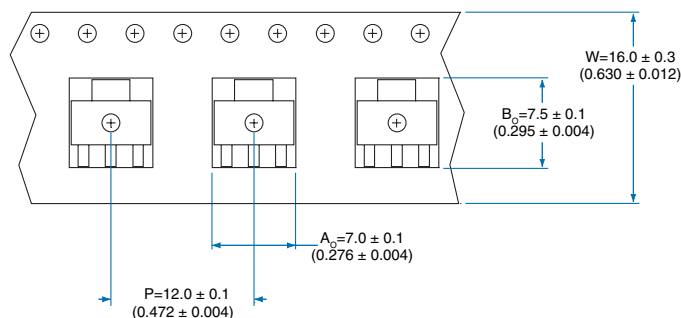
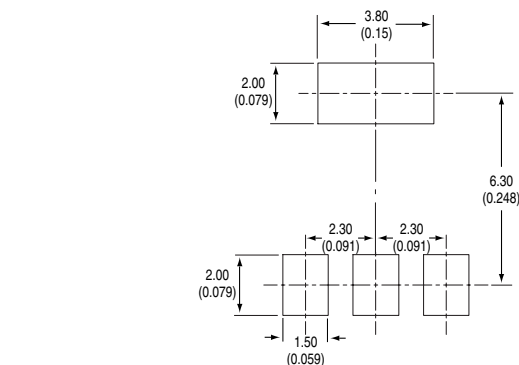
Soldering

Recommended soldering processes are limited to 245°C component body temperature for 10 seconds.

Note: Values are typical except where noted.

Technical drawing of a 35mm film reel. The drawing includes the following labels and dimensions:

- 330.2 DIA. (13.00 DIA.)**: Dimension for the outer diameter of the film reel.
- Top Cover Tape Thickness 0.102 MAX. (0.004 MAX.)**: Dimension for the thickness of the top cover tape.
- Embossed Carrier**: Label pointing to the carrier of the film.
- Embossment**: Label pointing to the embossed area on the film.
- $K_c = 1.956 \text{ MAX. (0.077 MAX.)}$** : Dimension for the embossed area.



NOTE: Tape dimensions not shown, comply with JEDEC Standard EIA-481-2

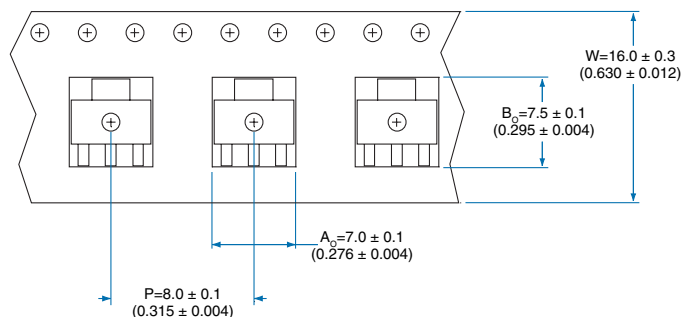
177.8 DIA.
(7.00 DIA.)

Top Cover
Tape Thickness
0.102 MAX.
(0.004 MAX.)

Embossed Carrier

Embossment

$K_c = 1.956 \text{ MAX.}$
(0.077 MAX.)



NOTE: Tape dimensions not shown, comply with JEDEC Standard EIA-481-2

DIMENSIONS:
mm
(inches)

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