



FEATURES

- Access time : 35/70ns (max.)
- Low power consumption :
 - Operating : 200 mW (typical)
 - Standby : 2.5mW (typical) Normal
 - 50μW (typical) L-version
 - 5μW (typical) LL-version
- Single 5V power supply
- All inputs and outputs TTL compatible
- Fully static operation
- Three state outputs
- Data retention voltage : 2V (min.)
- Package : 32-pin 600 mil PDIP
32-pin 450 mil SOP
32-pin 8x20mm TSOP-1

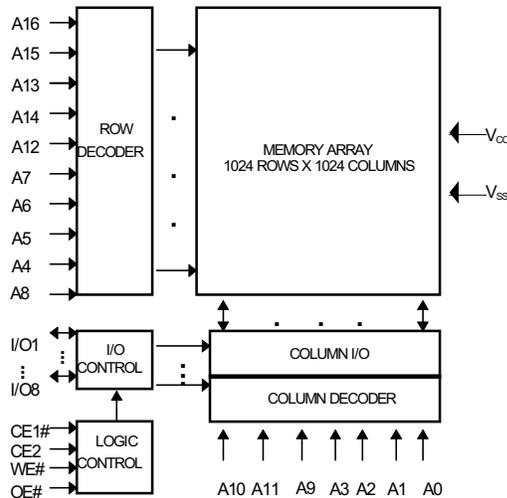
GENERAL DESCRIPTION

The UT621024 is a 1,048,576-bit low power CMOS static random access memory organized as 131,072 words by 8 bits. It is fabricated using high performance, high reliability CMOS technology.

The UT621024 is designed for low power application. It is particularly well suited for battery back-up nonvolatile memory application.

The UT621024 operates from a single 5V power supply and all inputs and outputs are fully TTL compatible.

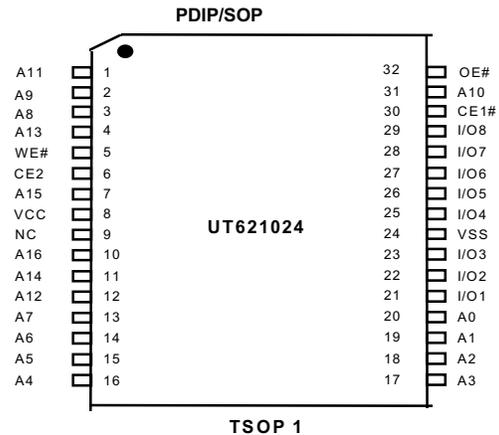
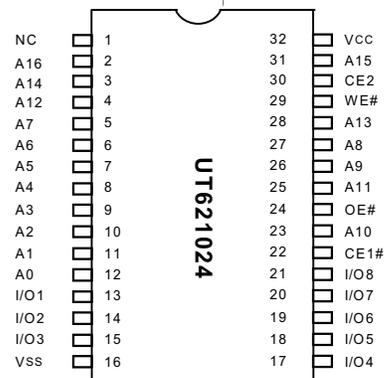
FUNCTIONAL BLOCK DIAGRAM



PIN DESCRIPTION

SYMBOL	DESCRIPTION
A0 - A16	Address Inputs
I/O1 - I/O8	Data Inputs/Outputs
CE1#, CE2	Chip Enable 1,2 Inputs
WE#	Write Enable Input
OE#	Output Enable Input
V _{CC}	Power Supply
V _{SS}	Ground
NC	No Connection

PIN CONFIGURATION



**ABSOLUTE MAXIMUM RATINGS***

PARAMETER	SYMBOL	RATING	UNIT
Terminal Voltage with Respect to V _{SS}	V _{TERM}	-0.5 to +7.0	V
Operating Temperature	T _A	0 to +70	°C
Temperature Under Bias	T _{BIAS}	-55 to +125	°C
Storage Temperature	T _{STG}	-65 to +150	°C
Power Dissipation	P _T	1	W
DC Output Current	I _{OUT}	50	mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to the absolute maximum rating conditions for extended period may affect device reliability.

TRUTH TABLE

MODE	CE1#	CE2	OE#	WE#	I/O OPERATION	SUPPLY CURRENT
Standby	H	X	X	X	High - Z	I _{SB} , I _{SB1}
Standby	X	L	X	X	High - Z	I _{SB} , I _{SB1}
Output Disable	L	H	H	H	High - Z	I _{CC}
Read	L	H	L	H	D _{OUT}	I _{CC}
Write	L	H	X	L	D _{IN}	I _{CC}

Note: H = V_{IH}, L = V_{IL}, X = Don't care.

DC ELECTRICAL CHARACTERISTICS (V_{CC} = 5V \pm 10%, T_A = 0°C to 70°C)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT	
Input High Voltage	V _{IH}		2.2	-	V _{CC} +0.5	V	
Input Low Voltage	V _{IL}		-0.5	-	0.8	V	
Input Leakage Current	I _{LI}	V _{SS} \leq V _{IN} \leq V _{CC}	-1	-	1	μ A	
Output Leakage Current	I _{LO}	V _{SS} \leq V _{IO} \leq V _{CC}	-1	-	1	μ A	
Output High Voltage	V _{OH}	I _{OH} = -1mA	2.4	-	-	V	
Output Low Voltage	V _{OL}	I _{OL} = 4mA	-	-	0.4	V	
DC Operating Power	I _{CC}	CE1# = V _{IL} , CE2 = V _{IH}	-	7	15	mA	
Average Operating	I _{CC1}	Cycle time = 1 μ s, 100% Dut	-	-	10	mA	
	I _{CC2}	Min.Cycle, 100% Duty, CE1# = V _{IL} , CE2 = V _{IH} , I _{IO} = 0mA	-35 -70	- -	60 40	100 70	mA mA
Standby Power	I _{SB}	CE1# = V _{IH} or CE2 = V _{IL}	Norma	-	-	10	mA
			-L	-	-	3	mA
			-LL	-	-	3	mA
Supply Current	I _{SB1}	CE1# \geq V _{CC} -0.2V or CE2 \leq 0.2V	Norma	-	0.5	5	mA
			-L	-	10	300*	μ A
			-LL	-	1	15*	μ A

*Those parameters are guaranteed by temperature range from 0°C to 50°C

**CAPACITANCE** ($T_A=25^{\circ}\text{C}$, $f=1.0\text{MHz}$)

PARAMETER	SYMBOL	MIN.	MAX.	UNIT
Input Capacitance	C_{IN}	-	8	pF
Input/Output Capacitance	$C_{I/O}$	-	10	pF

Note : These parameters are guaranteed by device characterization, but not production tested.

AC TEST CONDITIONS

Input Pulse Levels	0V to 3.0V
Input Rise and Fall Times	5ns
Input and Output Timing Reference Levels	1.5V
Output Load	$C_L=100\text{pF}$, $I_{OH}/I_{OL}=-1\text{mA}/4\text{mA}$

AC ELECTRICAL CHARACTERISTICS ($V_{CC} = 5V \pm 10\%$, $T_A = 0^{\circ}\text{C}$ to 70°C)**(1) READ CYCLE**

PARAMETER	SYMBOL	UT621024-35		UT621024-70		UNIT
		MIN.	MAX.	MIN.	MAX.	
Read Cycle Time	t_{RC}	35	-	70	-	ns
Address Access Time	t_{AA}	-	35	-	70	ns
Chip Enable Access Time	t_{ACE1} , t_{ACE2}	-	35	-	70	ns
Output Enable Access Time	t_{OE}	-	25	-	35	ns
Chip Enable to Output in Low-Z	t_{CLZ1}^* , t_{CLZ2}^*	10	-	10	-	ns
Output Enable to Output in Low-Z	t_{OLZ}^*	5	-	5	-	ns
Chip Disable to Output in High-Z	t_{CHZ1}^* , t_{CHZ2}^*	-	25	-	35	ns
Output Disable to Output in High-Z	t_{OHZ}^*	-	25	-	35	ns
Output Hold from Address Change	t_{OH}	5	-	5	-	ns

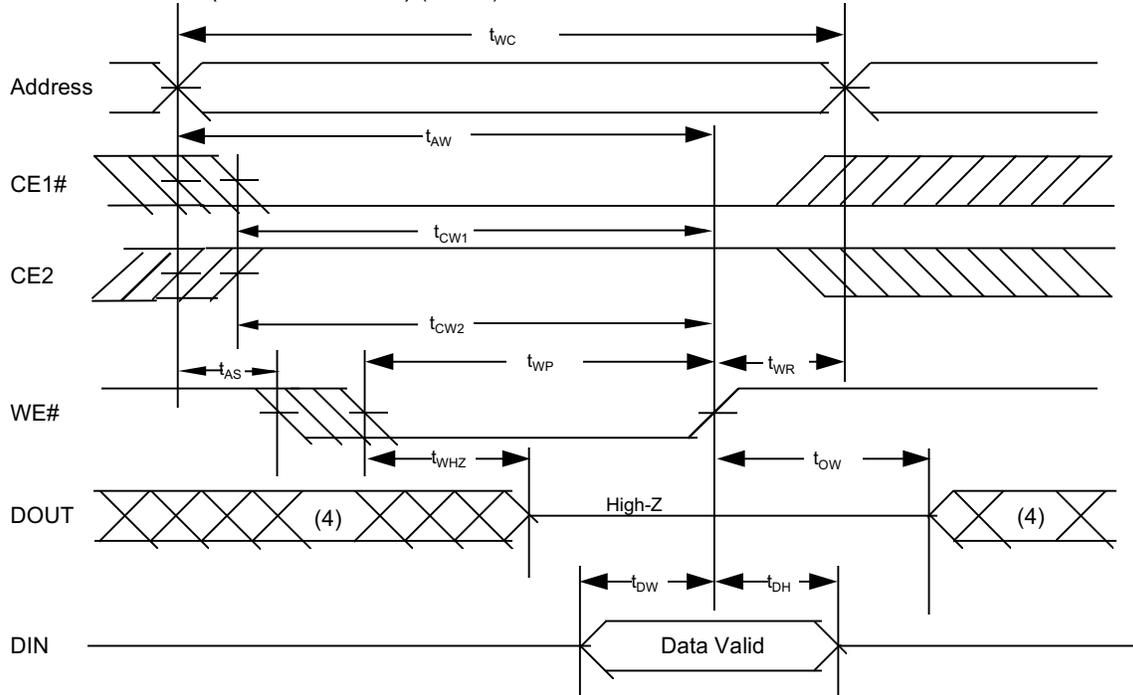
(2) WRITE CYCLE

PARAMETER	SYMBOL	UT621024-35		UT621024-70		UNIT
		MIN.	MAX.	MIN.	MAX.	
Write Cycle Time	t_{WC}	35	-	70	-	ns
Address Valid to End of Write	t_{AW}	30	-	60	-	ns
Chip Enable to End of Write	t_{CW1} , t_{CW2}	30	-	60	-	ns
Address Set-up Time	t_{AS}	0	-	0	-	ns
Write Pulse Width	t_{WP}	25	-	45	-	ns
Write Recovery Time	t_{WR}	0	-	0	-	ns
Data to Write Time Overlap	t_{DW}	20	-	30	-	ns
Data Hold from End of Write-Time	t_{DH}	0	-	0	-	ns
Output Active from End of Write	t_{OW}^*	5	-	5	-	ns
Write to Output in High-Z	t_{WHZ}^*	-	15	-	25	ns

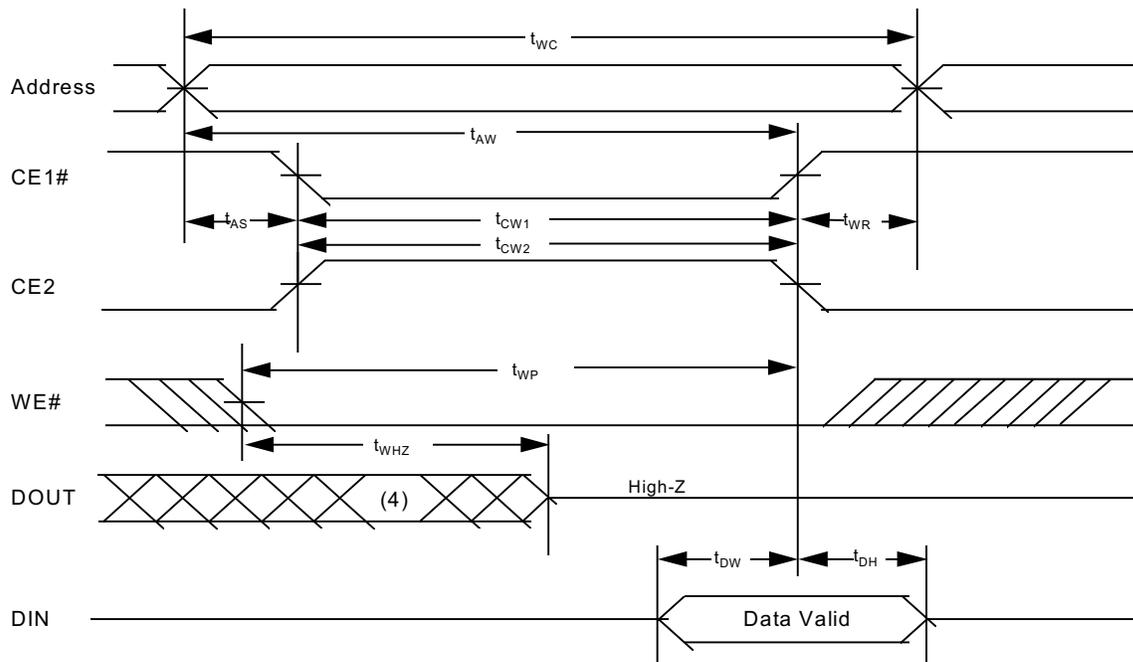
*These parameters are guaranteed by device characterization, but not production tested.



WRITE CYCLE 1 (WE# Controlled) (1,2,3,5)



WRITE CYCLE 2 (CE1# and CE2 Controlled) (1,2,5)





Notes :

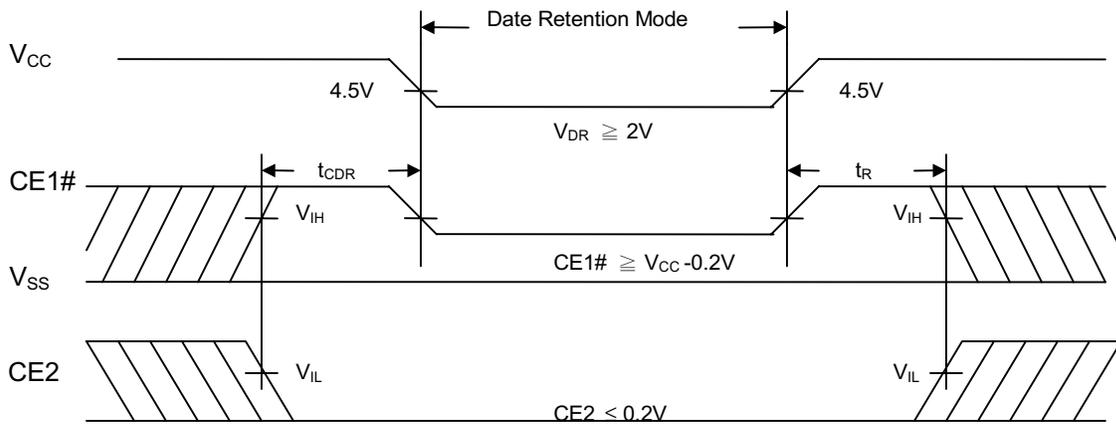
1. WE# or CE1# must be HIGH or CE2 must be LOW during all address transitions.
2. A write occurs during the overlap of a low CE1#, a high CE2 and a low WE#.
3. During a WE# controlled with write cycle with OE# LOW, t_{WP} must be greater than t_{WHZ}+t_{OW} to allow the I/O drivers to turn off and data to be placed on the bus.
4. During this period, I/O pins are in the output state, and input signals must not be applied.
5. If the CE1# LOW transition occurs simultaneously with or after WE# LOW transition, the outputs remain in a high impedance state.
6. t_{OW} and t_{WHZ} are specified with C_L=5pF. Transition is measured ± 500mV from steady state.

DATA RETENTION CHARACTERISTICS (TA = 0°C to 70°C)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT	
Vcc for Data Retention	V _{DR}	CE1# ≥ V _{CC} -0.2V or CE2 ≤ 0.2V	2.0	-	-	V	
Data Retention Current	I _{DR}	V _{CC} =3V CE1# ≥ V _{CC} -0.2V or CE2 ≤ 0.2V	- L	-	1	50	μA
			- LL	-	0.5	20	μA
Chip Disable to Data Retention Time	t _{CDR}	See Data Retention Waveforms (below)	0	-	-	ns	
Recovery Time	t _R		t _{RC} *	-	-	ns	

t_{RC}* = Read Cycle Time

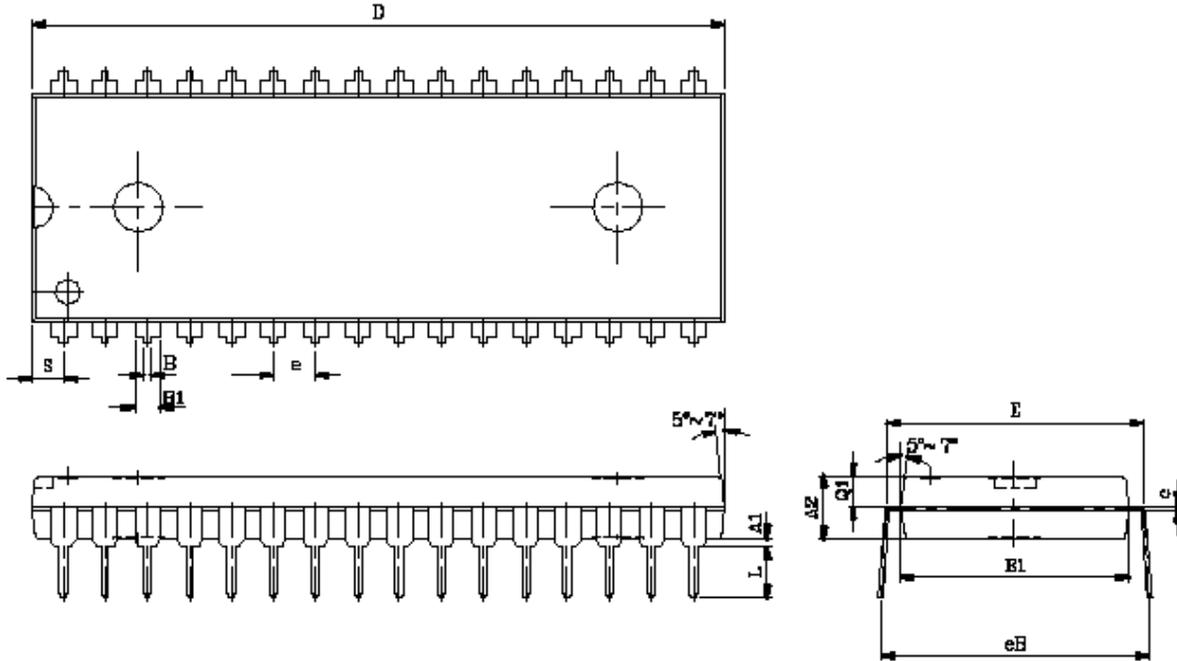
DATA RETENTION WAVEFORM





PACKAGE OUTLINE DIMENSION

32PIN 600 milPDIP PACKAGE OUTLINE DIMENSION

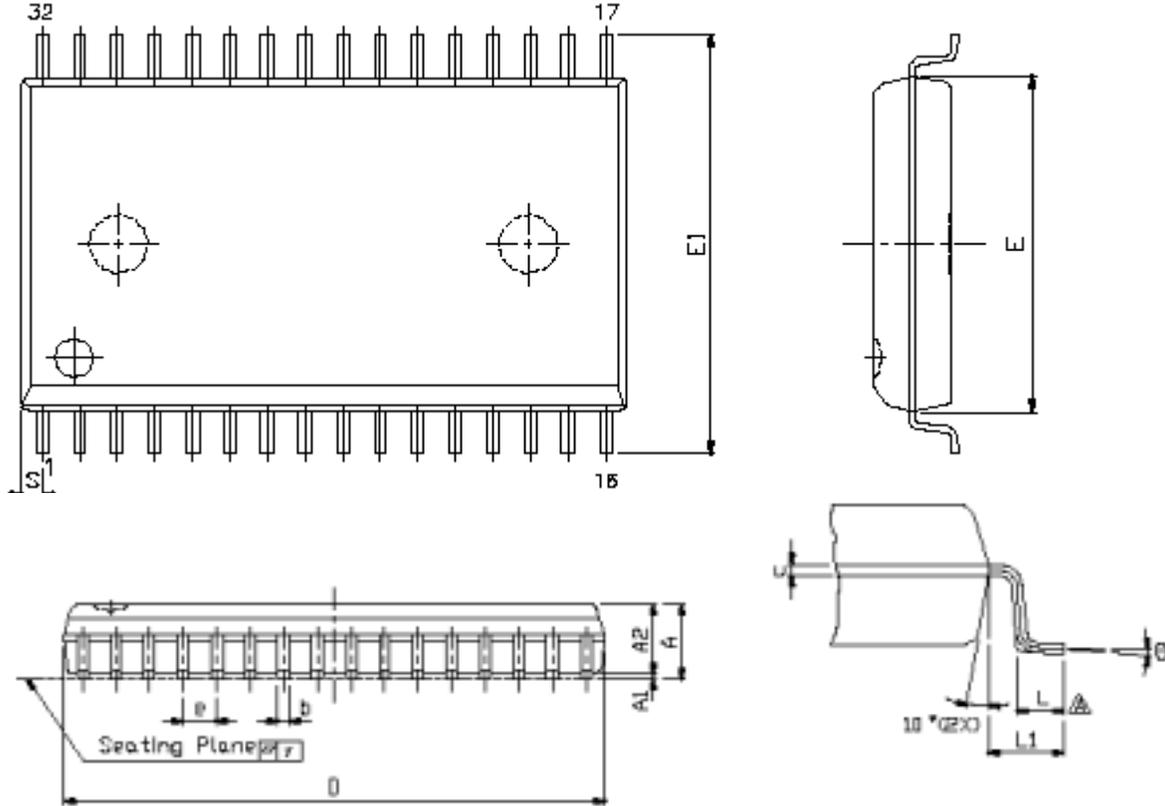


SYMBOL	UNIT	INCH(BASE)	MM(REF)
A1		0.010 (MIN)	0.254 (MIN)
A2		0.150 ± 0.005	3.810 ± 0.127
B		0.018 ± 0.005	0.457 ± 0.127
B1		0.050 ± 0.005	1.270 ± 0.127
c		0.010 ± 0.004	0.254 ± 0.102
D		1.650 ± 0.005	41.910 ± 0.127
E		0.600 ± 0.010	15.240 ± 0.254
E1		0.544 ± 0.004	13.818 ± 0.102
e		0.100(TYP)	2.540(TYP)
eB		0.640 ± 0.020	16.256 ± 0.508
L		0.130 ± 0.010	3.302 ± 0.254
S		0.075 ± 0.010	1.905 ± 0.254
Q1		0.070 ± 0.005	1.778 ± 0.127

Note: 1. D/E1/S DIMENSION DO NOT INCLUDE MOLD FLASH.



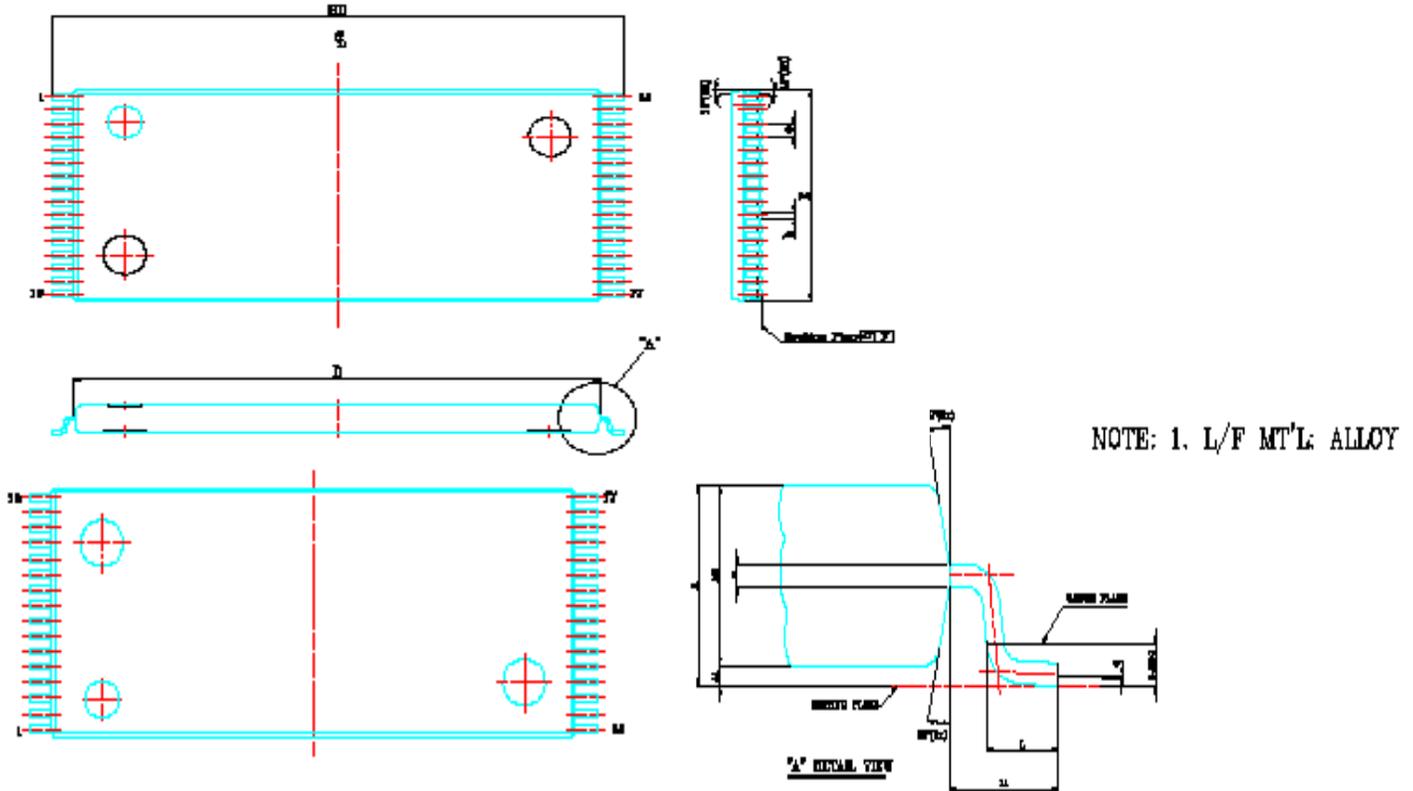
32pin 450mil SOP PACKAGE OUTLINE DIMENSION



SYMBOL	UNIT	INCH(BASE)	MM(REF)
A		0.118 (MAX)	2.997 (MAX)
A1		0.004(MIN)	0.102(MIN)
A2		0.111(MAX)	2.82(MAX)
b		0.016(TYP)	0.406(TYP)
c		0.008(TYP)	0.203(TYP)
D		0.817(MAX)	20.75(MAX)
E		0.445 ± 0.005	11.303 ± 0.127
E1		0.555 ± 0.005	11.303 ± 0.305
e		0.050(TYP)	1.270(TYP)
L		0.0347 ± 0.008	0.881 ± 0.203
L1		0.055 ± 0.008	1.397 ± 0.203
S		0.026(MAX)	0/914 (MAX)
y		0.004(MAX)	0.101(MAX)
θ		0° -10°	0° -10°



32pin TSOP-I PACKAGE OUTLINE DIMENSION



SYMBOL	UNIT	INCH(BASE)	MM(REF)
A		0.047 (MAX)	1.20 (MAX)
A1		0.004 ± 0.002	0.10 ± 0.05
A2		0.039 ± 0.002	1.00 ± 0.05
b		0.008 + 0.002 - 0.001	0.20 + 0.05 - 0.03
c		0.005 (TYP)	0.127 (TYP)
D		0.724 ± 0.004	18.40 ± 0.10
E		0.315 ± 0.004	8.00 ± 0.10
e		0.020 (TYP)	0.50 (TYP)
HD		0.787 ± 0.008	20.00 ± 0.20
L		0.0197 ± 0.004	0.50 ± 0.10
L1		0.0315 ± 0.004	0.08 ± 0.10
y		0.003 (MAX)	0.076 (MAX)
θ		0°~5°	0°~5°



UTRON

UT621024

Rev. 1.2

128K X 8 BIT LOW POWER CMOS SRAM

ORDERING INFORMATION

PART NO.	ACCESS TIME (ns)	STANDBY CURRENT (μ A)	PACKAGE
UT621024PC-70	70	5000	32PIN PDIP
UT621024PC-70L	70	300	32PIN PDIP
UT621024PC-70LL	70	15	32PIN PDIP
UT621024PC-70	70	5000	32PIN SOP
UT621024SC-70L	70	300	32PIN SOP
UT621024SC-70LL	70	15	32PIN SOP
UT621024LC-70	70	5000	32PIN TSOP-I
UT621024LC-70L	70	300	32PIN TSOP-I
UT621024LC-70LL	70	15	32PIN TSOP-I