

# Medium-Power Plastic PNP Silicon Transistors

... designed for driver circuits, switching, and amplifier applications. These high-performance plastic devices feature:

- Low Saturation Voltage —  
 $V_{CE(sat)} = 0.6 \text{ Vdc (Max) @ } I_C = 1.0 \text{ Amp}$
- Excellent Power Dissipation Due to Thermopad Construction —  
 $P_D = 30 \text{ W @ } T_C = 25^\circ\text{C}$
- Excellent Safe Operating Area
- Gain Specified to  $I_C = 1.0 \text{ Amp}$
- Complement to NPN 2N4921, 2N4922, 2N4923

## \*MAXIMUM RATINGS

Ratings	Symbol	2N4918	2N4919	2N4920	Unit
Collector-Emitter Voltage	$V_{CEO}$	40	60	80	Vdc
Collector-Base Voltage	$V_{CB}$	40	60	80	Vdc
Emitter-Base Voltage	$V_{EB}$	5.0			Vdc
Collector Current — Continuous (1)	$I_C^*$	1.0 3.0			A dc
Base Current	$I_B$	1.0			A dc
Total Power Dissipation @ $T_C = 25^\circ\text{C}$ Derate above $25^\circ\text{C}$	$P_D$	30 0.24			Watts W/ $^\circ\text{C}$
Operating & Storage Junction Temperature Range	$T_J, T_{stg}$	-65 to +150			$^\circ\text{C}$

## THERMAL CHARACTERISTICS (2)

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$\theta_{JC}$	4.16	$^\circ\text{C/W}$

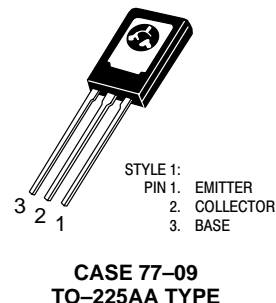
\*Indicates JEDEC Registered Data for 2N4918 Series.

- (1) The 1.0 Amp maximum  $I_C$  value is based upon JEDEC current gain requirements. The 3.0 Amp maximum value is based upon actual current-handling capability of the device (See Figure 5).
- (2) Recommend use of thermal compound for lowest thermal resistance.

**2N4918  
thru  
2N4920\***

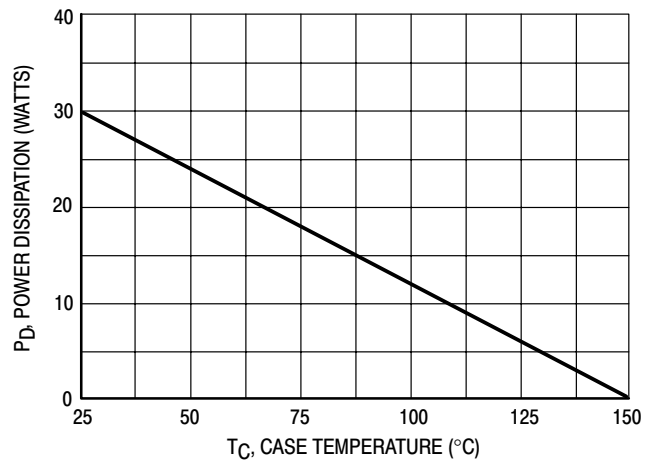
\*ON Semiconductor Preferred Device

**3 AMPERE  
GENERAL-PURPOSE  
POWER TRANSISTORS  
40-80 VOLTS  
30 WATTS**



Preferred devices are ON Semiconductor recommended choices for future use and best overall value.

## 2N4918 thru 2N4920



**Figure 1. Power Derating**

# 2N4918 thru 2N4920

## ELECTRICAL CHARACTERISTICS ( $T_C = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
<b>OFF CHARACTERISTICS</b>				
Collector–Emitter Sustaining Voltage (1) ( $I_C = 0.1 \text{ A dc}$ , $I_B = 0$ )	$V_{CEO(sus)}$	40 60 80	—	Vdc
Collector Cutoff Current ( $V_{CE} = 20 \text{ Vdc}$ , $I_B = 0$ ) ( $V_{CE} = 30 \text{ Vdc}$ , $I_B = 0$ ) ( $V_{CE} = 40 \text{ Vdc}$ , $I_B = 0$ )	$I_{CEO}$	— — —	0.5 0.5 0.5	mAdc
Collector Cutoff Current ( $V_{CE} = \text{Rated } V_{CEO}$ , $V_{BE(off)} = 1.5 \text{ Vdc}$ ) ( $V_{CE} = \text{Rated } V_{CEO}$ , $V_{BE(off)} = 1.5 \text{ Vdc}$ , $T_C = 125^\circ\text{C}$ )	$I_{CEX}$	— —	0.1 0.5	mAdc
Collector Cutoff Current ( $V_{CB} = \text{Rated } V_{CB}$ , $I_E = 0$ )	$I_{CBO}$	—	0.1	mAdc
Emitter Cutoff Current ( $V_{BE} = 5.0 \text{ Vdc}$ , $I_C = 0$ )	$I_{EBO}$	—	1.0	mAdc

## ON CHARACTERISTICS

DC Current Gain (1) ( $I_C = 50 \text{ mAdc}$ , $V_{CE} = 1.0 \text{ Vdc}$ ) ( $I_C = 500 \text{ mAdc}$ , $V_{CE} = 1.0 \text{ Vdc}$ ) ( $I_C = 1.0 \text{ A dc}$ , $V_{CE} = 1.0 \text{ Vdc}$ )	$h_{FE}$	40 30 10	— 150 —	—
Collector–Emitter Saturation Voltage (1) ( $I_C = 1.0 \text{ A dc}$ , $I_B = 0.1 \text{ A dc}$ )	$V_{CE(sat)}$	—	0.6	Vdc
Base–Emitter Saturation Voltage (1) ( $I_C = 1.0 \text{ A dc}$ , $I_B = 0.1 \text{ A dc}$ )	$V_{BE(sat)}$	—	1.3	Vdc
Base–Emitter On Voltage (1) ( $I_C = 1.0 \text{ A dc}$ , $V_{CE} = 1.0 \text{ Vdc}$ )	$V_{BE(on)}$	—	1.3	Vdc

## SMALL–SIGNAL CHARACTERISTICS

Current–Gain — Bandwidth Product ( $I_C = 250 \text{ mAdc}$ , $V_{CE} = 10 \text{ Vdc}$ , $f = 1.0 \text{ MHz}$ )	$f_T$	3.0	—	MHz
Output Capacitance ( $V_{CB} = 10 \text{ Vdc}$ , $I_E = 0$ , $f = 100 \text{ kHz}$ )	$C_{ob}$	—	100	pF
Small–Signal Current Gain ( $I_C = 250 \text{ mAdc}$ , $V_{CE} = 10 \text{ Vdc}$ , $f = 1.0 \text{ kHz}$ )	$h_{fe}$	25	—	—

\*Indicates JEDEC Registered Data.

(1) Pulse Test:  $PW \approx 300 \mu\text{s}$ , Duty Cycle  $\approx 2.0\%$

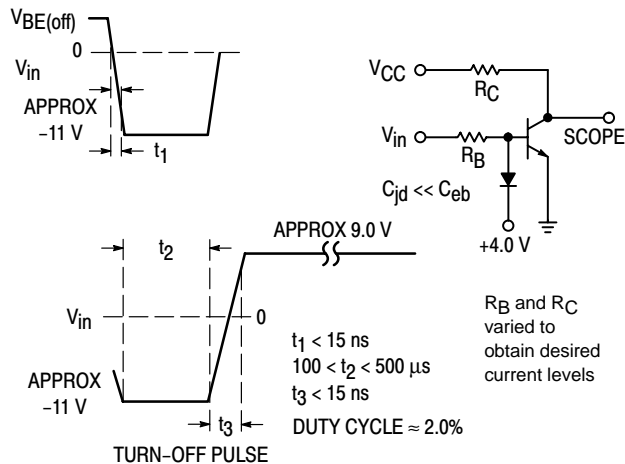


Figure 2. Switching Time Equivalent Test Circuit

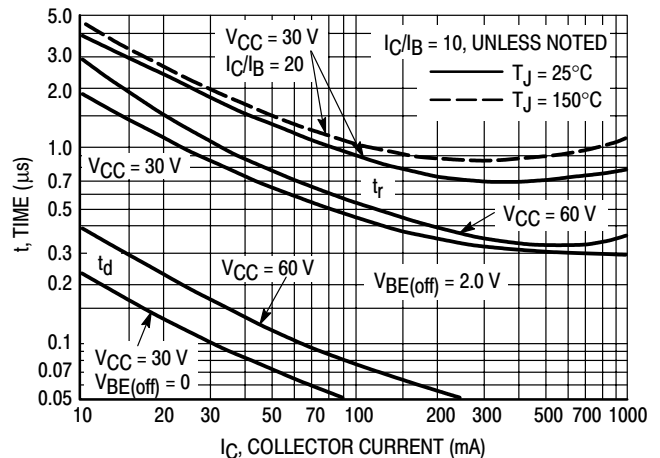
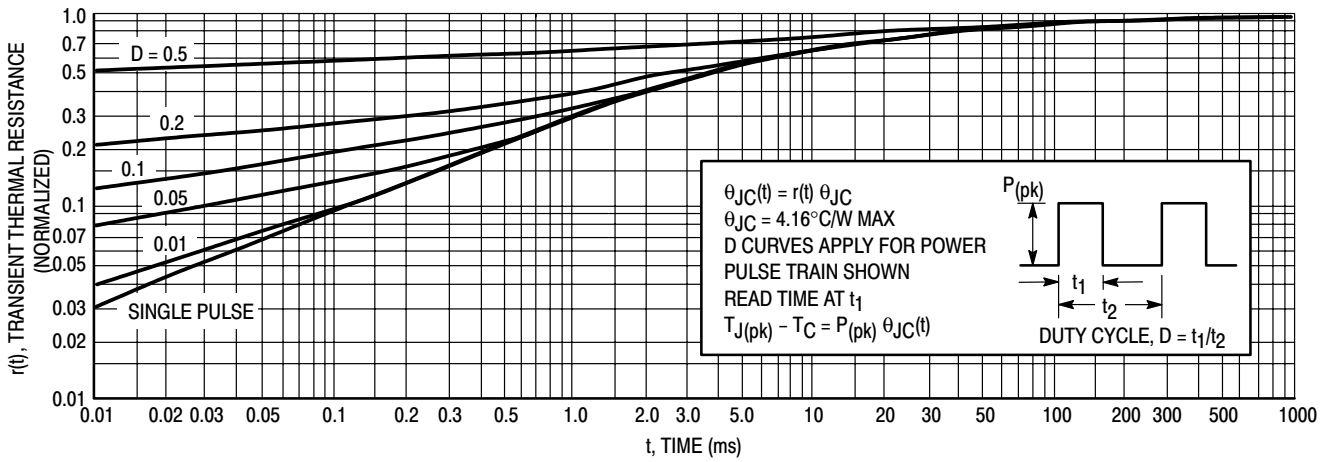
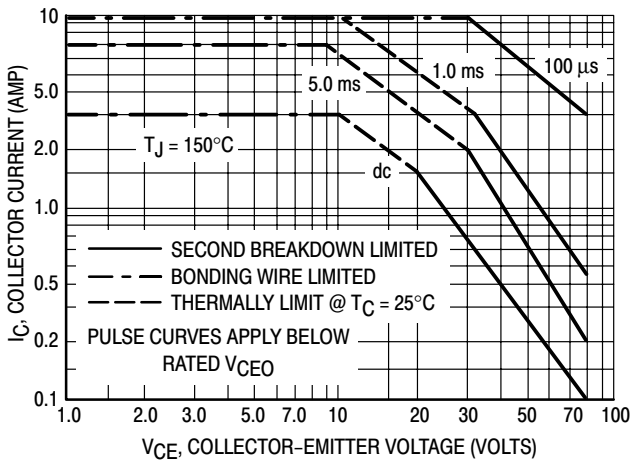


Figure 3. Turn-On Time

## 2N4918 thru 2N4920



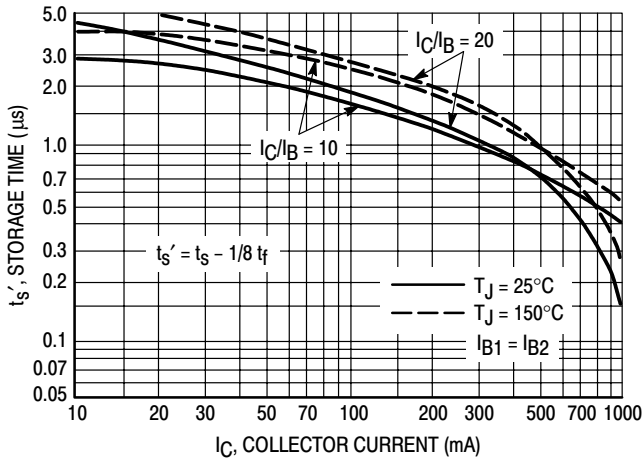
**Figure 4. Thermal Response**



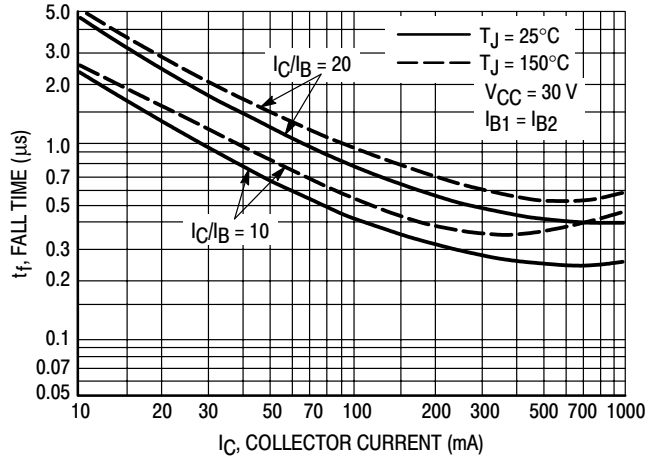
**Figure 5. Active-Region Safe Operating Area**

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate  $I_C - V_{CE}$  operation i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 5 is based on  $T_{J(pk)} = 150^{\circ}\text{C}$ ;  $T_C$  is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided  $T_{J(pk)} \leq 150^{\circ}\text{C}$ . At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.



**Figure 6. Storage Time**



**Figure 7. Fall Time**

TYPICAL DC CHARACTERISTICS

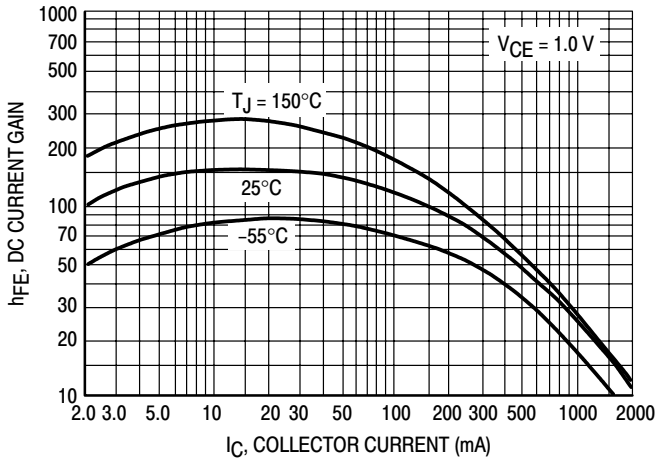


Figure 8. Current Gain

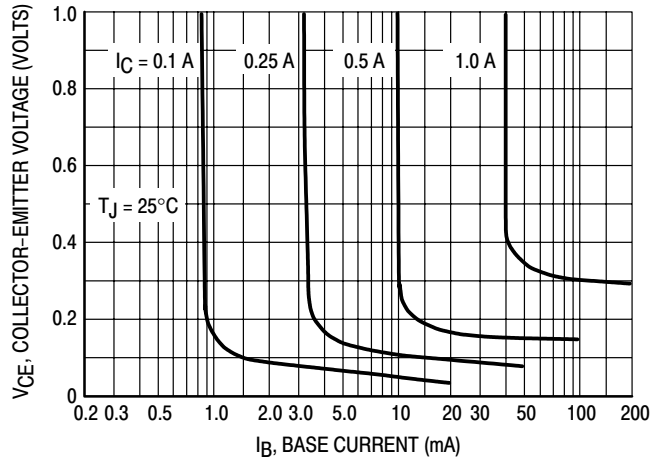


Figure 9. Collector Saturation Region

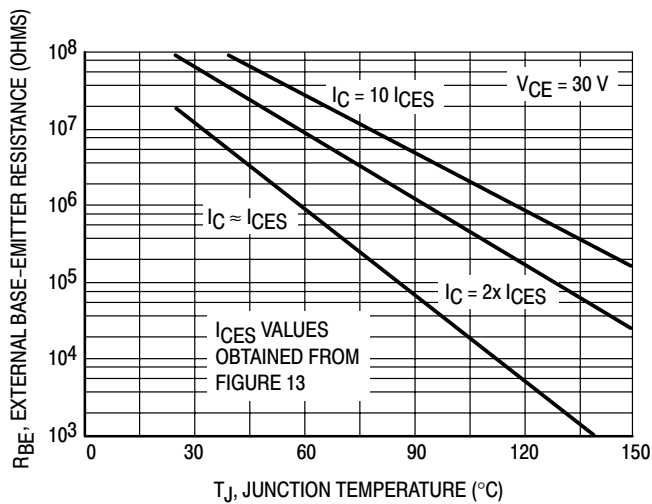


Figure 10. Effects of Base-Emitter Resistance

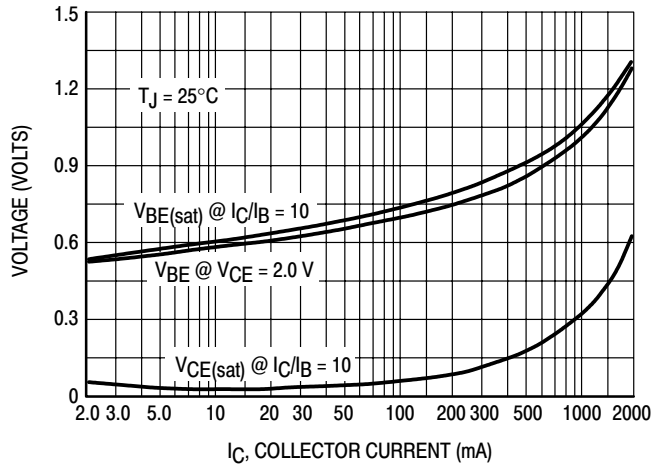


Figure 11. "On" Voltage

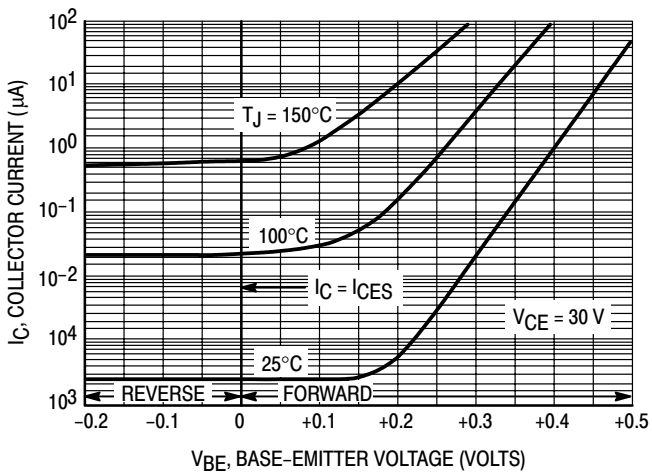


Figure 12. Collector Cut-Off Region

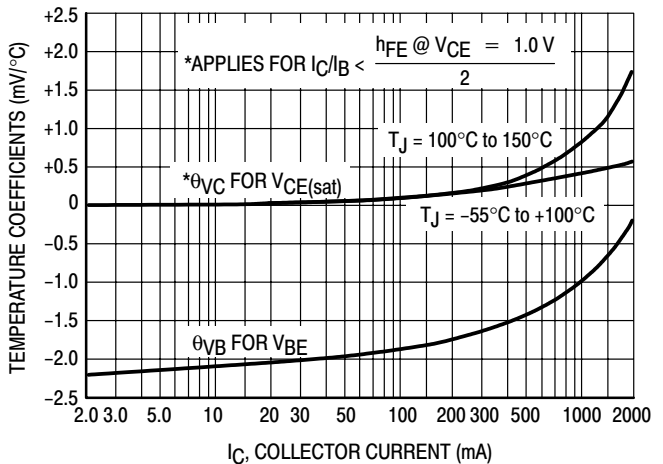
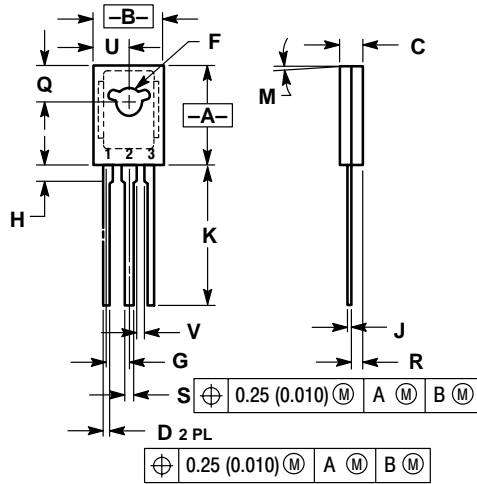


Figure 13. Temperature Coefficients

# 2N4918 thru 2N4920

## PACKAGE DIMENSIONS

TO-225AA  
CASE 77-09  
ISSUE W



- NOTES:  
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.  
2. CONTROLLING DIMENSION: INCH.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.425	0.435	10.80	11.04
B	0.295	0.305	7.50	7.74
C	0.095	0.105	2.42	2.66
D	0.020	0.026	0.51	0.66
F	0.115	0.130	2.93	3.30
G	0.094 BSC		2.39 BSC	
H	0.050	0.095	1.27	2.41
J	0.015	0.025	0.39	0.63
K	0.575	0.655	14.61	16.63
M	5° TYP		5° TYP	
Q	0.148	0.158	3.76	4.01
R	0.045	0.065	1.15	1.65
S	0.025	0.035	0.64	0.88
U	0.145	0.155	3.69	3.93
V	0.040	---	1.02	---

- STYLE 1:  
PIN 1. EMITTER  
2. COLLECTOR  
3. BASE

## Notes

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