FAIRCHILD SEMICONDUCTOR®

June 2006

FDZ191P

P-Channel 1.5V Specified PowerTrench™ WL-CSP MOSFET

General Description

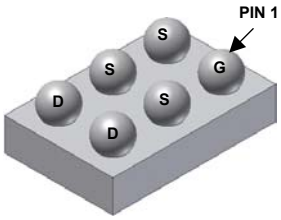
Designed on Fairchild's advanced 1.5V PowerTrench process with state of the art "low pitch" WLCSP packaging process, the FDZ191P minimizes both PCB space and $R_{DS(ON)}$. This advanced WLCSP MOSFET embodies a breakthrough in packaging technology which enables the device to combine excellent thermal transfer characteristics, ultra-low profile packaging, low gate charge, and low $R_{DS(ON)}$.

Applications

- Battery management
- Load switch
- Battery protection

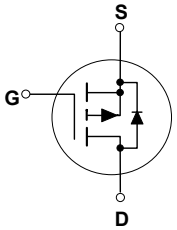
Features

- –1A, –20 V $R_{DS(ON)}$ = 85 mΩ @ V_{GS} = –4.5 V
  $R_{DS(ON)}$ = 123 mΩ @ V_{GS} = –2.5 V
  $R_{DS(ON)}$ = 200 mΩ @ V_{GS} = –1.5 V
- Occupies only 1.5 mm^2 of PCB area
  Less than 50% of the area of 2 x 2 BGA
- Ultra-thin package: less than 0.65 mm height when mounted to PCB
- High power and current handling capability



BOTTOM

TOP



Absolute Maximum Ratings

T_A=25°C unless otherwise noted

Symbol	Parameter		Ratings	Units
V_{DSS}	Drain-Source Voltage		–20	V
V_{GSS}	Gate-Source Voltage		± 8	V
I_D	Drain Current – Continuous	(Note 1a)	–3	A
	– Pulsed		–15	
P_D	Power Dissipation (Steady State)	(Note 1a)	1.5	W
		(Note 1b)	0.9	
T_J, T_{stg}	Operating and Storage Junction Temperature Range		–55 to +150	°C

Thermal Characteristics

$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	(Note 1a)	83	°C/W
		(Note 1b)	140	

Package Marking and Ordering Information

Device Marking	Device	Reel Size	Tape width	Quantity
1	FDZ191P	7"	8mm	3000

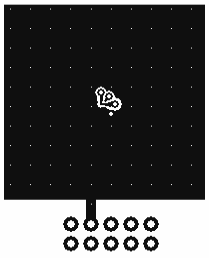
Electrical Characteristics

T_A = 25°C unless otherwise noted

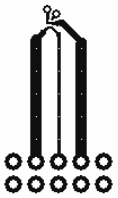
Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
Off Characteristics						
BV_{DSS}	Drain–Source Breakdown Voltage	V_{GS} = 0 V, I_D = –250 μA	–20			V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	I_D = –250 μA, Referenced to 25°C		–12		mV/°C
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = –16 V, V_{GS} = 0 V			–1	μA
I_{GSS}	Gate–Body Leakage Current, Reverse	V_{GS} = ± 8 V, V_{DS} = 0 V			±100	nA
On Characteristics (Note 2)						
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS} = V_{GS}, I_D = –250 μA	–0.4	–0.6	–1.5	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate Threshold Voltage Temperature Coefficient	I_D = –250 μA,Referenced to 25°C		2		mV/°C
$R_{DS(on)}$	Static Drain–Source On–Resistance	V_{GS} = –4.5 V, I_D = –1 A V_{GS} = –2.5 V, I_D = –1 A V_{GS} = –1.5 V, I_D = –1 A V_{GS} = –4.5 V,I_D = –1 A T_J=125°C		67 85 140 87	85 123 200 123	mΩ
$I_{D(on)}$	On–State Drain Current	V_{GS} = –4.5 V, V_{DS} = –5 V	–10			A
g_{FS}	Forward Transconductance	V_{DS} = –5 V, I_D = –1 A		7		S
Dynamic Characteristics						
C_{iss}	Input Capacitance	V_{DS} = –10 V, V_{GS} = 0 V, f = 1.0 MHz		800		pF
C_{oss}	Output Capacitance			155		pF
C_{rss}	Reverse Transfer Capacitance			90		pF
R_G	Gate Resistance	f = 1.0 MHz		9		Ω
Switching Characteristics (Note 2)						
$t_{d(on)}$	Turn–On Delay Time	V_{DD} = –10 V, I_D = –1 A, V_{GS} = –4.5 V, R_{GEN} = 6		11	20	ns
t_r	Turn–On Rise Time			10	20	ns
$t_{d(off)}$	Turn–Off Delay Time			50	80	ns
t_f	Turn–Off Fall Time			30	48	ns
Q_g	Total Gate Charge	V_{DS} = –10 V, I_D = –1 A, V_{GS} = –4.5 V		9	13	nC
Q_{gs}	Gate–Source Charge			1		nC
Q_{gd}	Gate–Drain Charge			2		nC
Drain–Source Diode Characteristics and Maximum Ratings						
I_S	Maximum Continuous Drain–Source Diode Forward Current				–1.1	A
V_{SD}	Drain–Source Diode Forward Voltage	V_{GS} = 0 V, I_S = –1.1 A (Note 2)		–0.7	–1.2	V
trr	Diode Reverse Recovery Time	IF = -1A, diF/dt = 100 A/μs		21		nS
Qrr	Diode Reverse Recovery Charge			5		nC

Notes:

1. $R_{\theta JA}$ is determined with the device mounted on a 1 in² 2 oz. copper pad on a 1.5 x 1.5 in. board of FR-4 material. The thermal resistance from the junction to the circuit board side of the solder ball, $R_{\theta JB}$, is defined for reference. For $R_{\theta JC}$, the thermal reference point for the case is defined as the top surface of the copper chip carrier. $R_{\theta JC}$ and $R_{\theta JB}$ are guaranteed by design while $R_{\theta JA}$ is determined by the user's board design.



a) 83 °C/W when mounted on a 1in² pad of 2 oz copper, 1.5” x 1.5” x 0.062” thick PCB

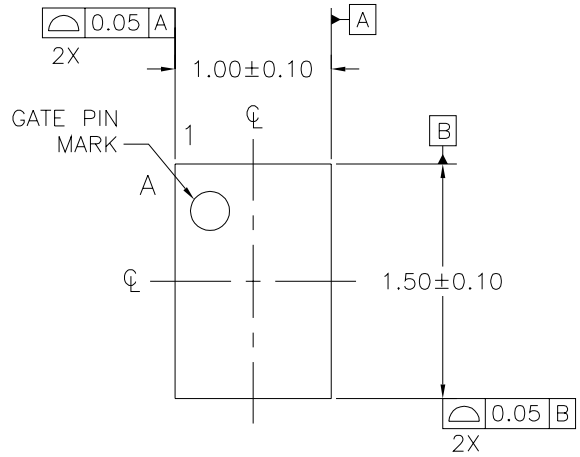


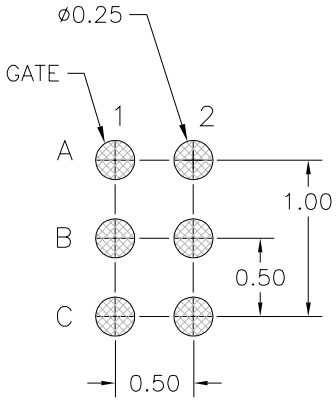
b) 140 °C/W when mounted on a minimum pad of 2 oz copper

Scale 1 : 1 on letter size paper

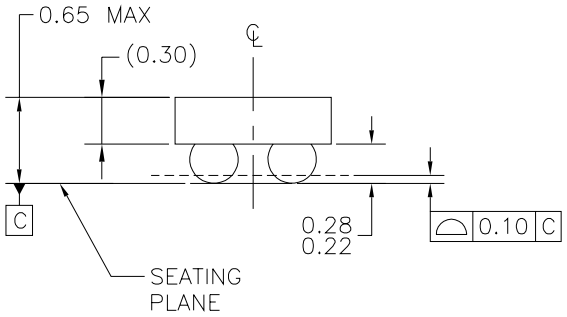
2. Pulse Test: Pulse Width < 300μs, Duty Cycle < 2.0%

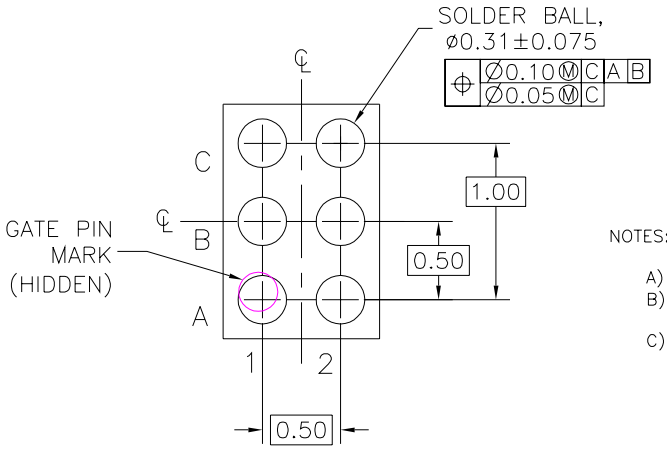
Dimensional Pad and Layout





LAND PATTERN RECOMMENDATION





NOTES: UNLESS OTHERWISE SPECIFIED

A) ALL DIMENSIONS ARE IN MILLIMETERS.
B) NO JEDEC REGISTRATION REFERENCE AS OF OCTOBER 2005.
C) TERMINAL CONFIGURATION TABLE.

POSITION	DESIGNATION
C1, C2	DRAIN
A1	GATE
A2, B1, B2	SOURCE

UC006AAREVB

Typical Characteristics

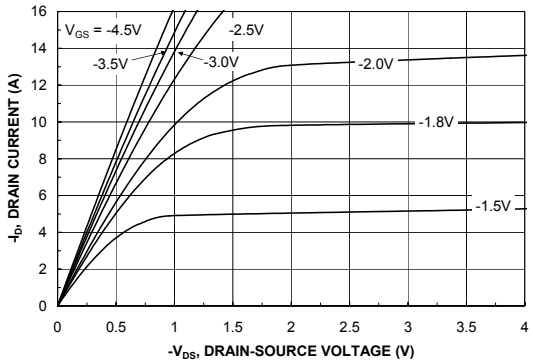


Figure 1. On-Region Characteristics.

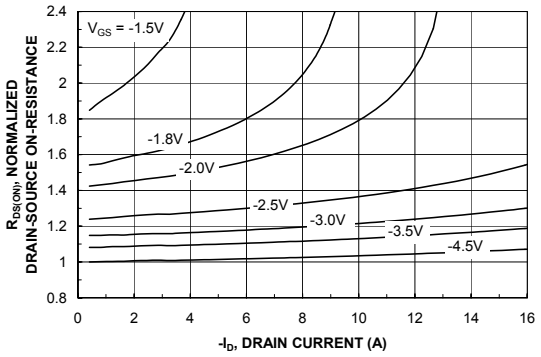


Figure 2. On-Resistance Variation with Drain Current and Gate Voltage.

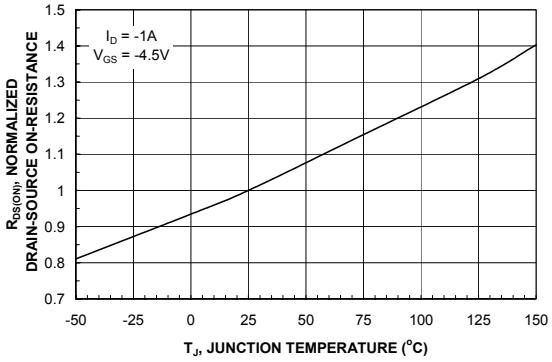


Figure 3. On-Resistance Variation with Temperature.

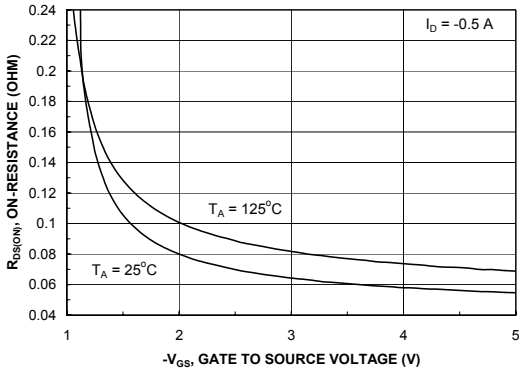


Figure 4. On-Resistance Variation with Gate-to-Source Voltage.

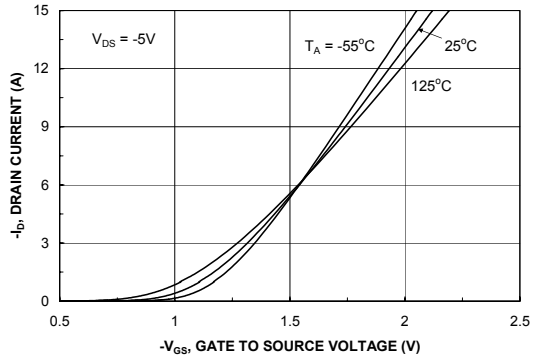


Figure 5. Transfer Characteristics.

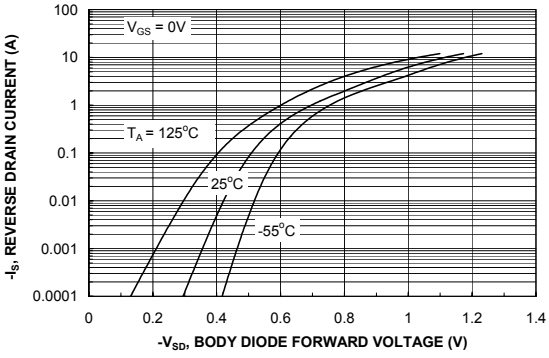


Figure 6. Body Diode Forward Voltage Variation with Source Current and Temperature.

Typical Characteristics

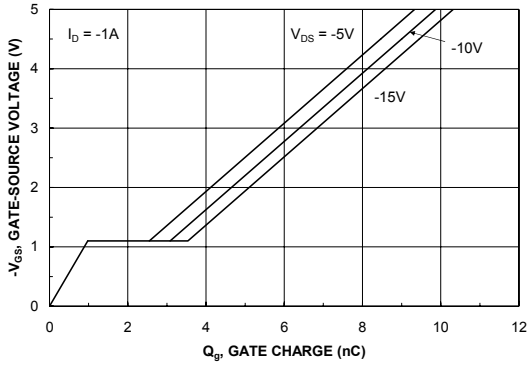


Figure 7. Gate Charge Characteristics.

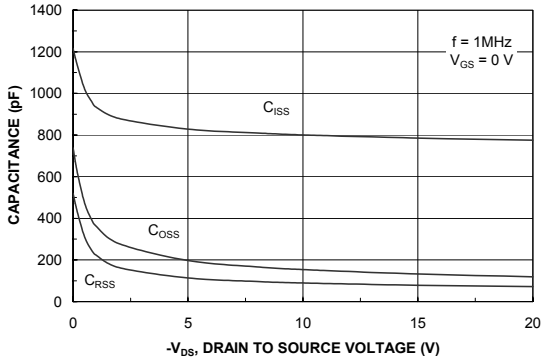


Figure 8. Capacitance Characteristics.

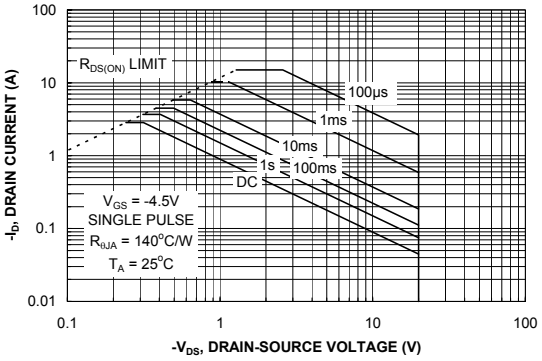


Figure 9. Maximum Safe Operating Area.

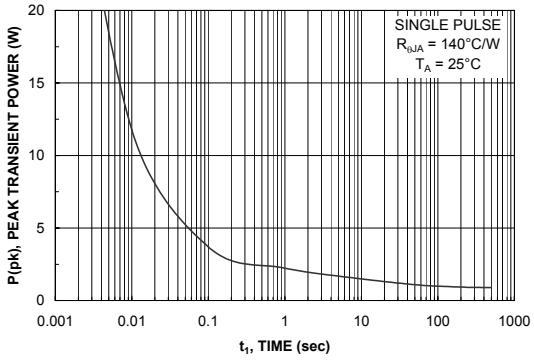


Figure 10. Single Pulse Maximum Power Dissipation.

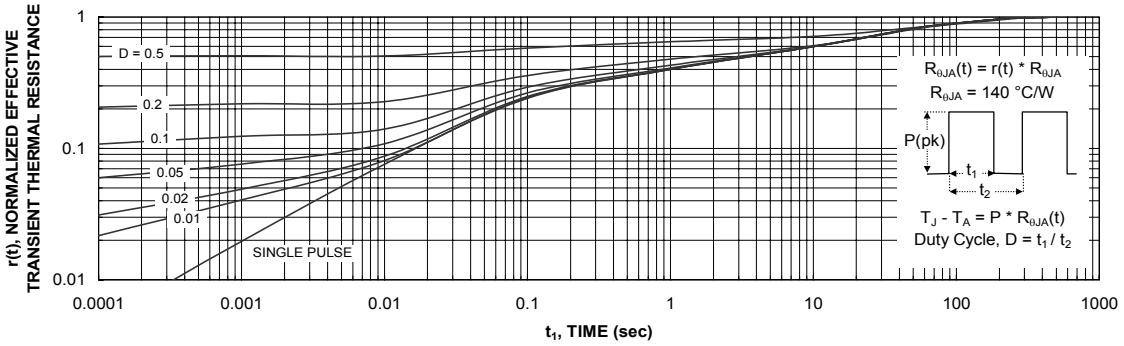


Figure 11. Transient Thermal Response Curve.

Thermal characterization performed using the conditions described in Note 1b.
Transient thermal response will change depending on the circuit board design.